User's Guide

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For Safety Information, Warranties, and Regulatory Information, see the pages at the end of this manual.

HP E2415B Analysis Probe for 8051-Compatible Microcontrollers

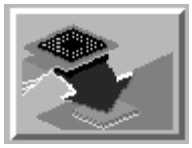
The HP E2415B Analysis Probe — At a Glance

The HP E2415B Analysis Probe provides a complete interface for state or timing analysis between any 8051-compatible microcontroller and HP logic analyzers. These logic analyzers support various combinations of mixed state/timing analysis. The supported logic analyzers are listed in chapters 1.

A microcontroller is defined as compatible if it conforms to the 8051 architecture, uses the 8051 instruction set, and uses the 40-pin DIP or 44-pin PLCC pinout. This covers a large number of products from Intel, Philips, MHS, Dallas, Siemans, and SMC.

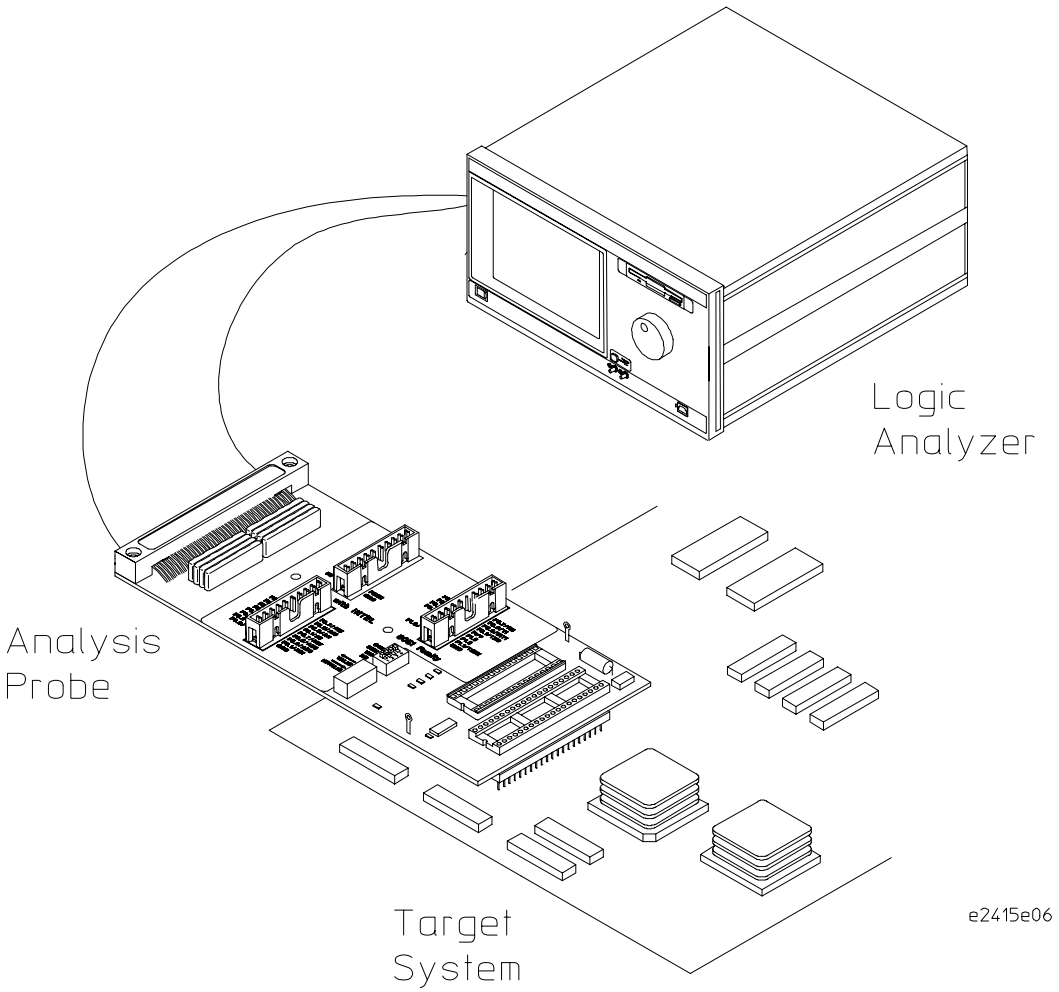
The HP E2415B also contains a socket for accepting a 64K, 128K, 256K, or 512K programmable memory. This socket allows any microcontroller internal memory to be mapped to external.

The analysis probe provides the physical connection between the target microcontroller and the logic analyzer. The 8051 configuration software sets up the format specification menu of the logic analyzer for compatibility with the 8051 microcontrollers. The inverse assemblers allow you to obtain displays of 8051 code execution in 8051 assembly language mnemonics.



If you are using the analysis probe with the HP 16600 or HP 16700 series logic analysis systems, you only need this manual as a reference. The HP 16600 and 16700 series contain a Setup Assistant, which guides you through the connection and configuration process using on-screen dialog windows. For an overview of Setup Assistant, refer to Chapter 1, "Setup Assistant."

For more information on the logic analyzers or microcontroller, refer to the appropriate reference manuals for those products.

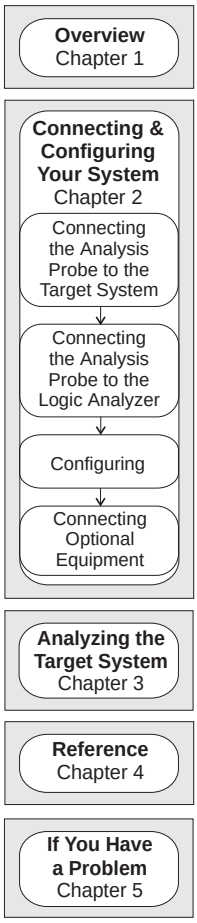


Analyzing a Target System with the HP E2415B Analysis Probe

In This Book

This book is the User's Guide for the HP E2415B Analysis Probe. It assumes that you have a working knowledge of the logic analyzer used and the microcontroller being analyzed.

This user's guide is organized into the following chapters:



Chapter 1 contains overview information, including a list of required equipment.

Chapter 2 explains how to connect the logic analyzer to your target system through the analysis probe, and how to configure the analysis probe and logic analyzer to interpret target system activity. The last section in this chapter shows you how to hook up optional equipment to obtain additional functionality.

HP 16600 and HP 16700 Series Logic Analysis Systems

If you are using the analysis probe with HP 16600 or HP 16700 series logic analysis systems, you only need this manual as a reference for obtaining and interpreting data. The HP 16600 and HP 16700 contain a Setup Assistant, which guides you through the connection and configuration process using on-screen dialog windows. For an overview of Setup Assistant, refer to chapter 1, "Setup Assistant."

Chapter 3 provides information on analyzing the supported microcontrollers.

Chapter 4 contains reference information on the analysis probe.

Chapter 5 contains troubleshooting information.

Contents

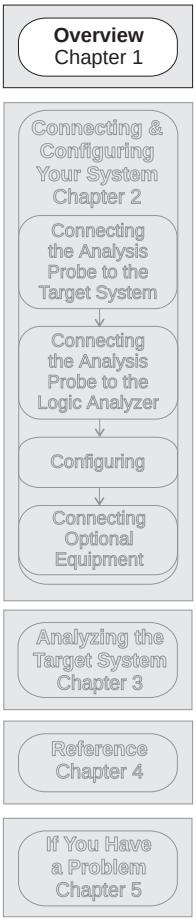
1

Overview

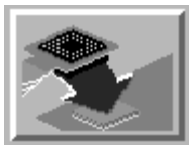
Overview

This chapter describes:

- Setup Assistant
- Logic analyzers supported
- Logic analyzer software version requirements
- Equipment used with the analysis probe
- Equipment supplied
- Minimum equipment required
- Additional equipment supported



Setup Assistant



Setup Assistant is an online tool for connecting and configuring your logic analysis system for microprocessor and bus analysis. Setup Assistant is available on the HP 16600 and HP 16700 series logic analysis systems. You can use Setup Assistant in place of the connection and configuration procedures provided in chapter 2.

This menu-driven tool will guide you through the connection procedures for connecting the logic analyzer to an analysis probe, an emulation module, or other supported equipment. It will also guide you through connecting an analysis probe to the target system.

Access Setup Assistant by clicking its icon in the Logic Analysis System window. The on-screen dialog prompts you to choose the type of measurements you want to make, the type of target system, and the associated products that you want to set up.

If you ordered this product with your HP 16600/700 logic analysis system, the logic analysis system has the latest software installed, including support for this product. If you received this product after you received your logic analysis system, this product might not be listed under supported products. In that case, you need to install the I8051 Processor Support Package. Use the procedure on the CD-ROM jacket to install the I8051 Processor Support Package.

Logic Analyzers Supported

The table below lists the logic analyzers supported by the HP E2415B Analysis Probe. Logic analyzer software version requirements are shown on the following page.

The HP E2415B requires three logic analyzer pods (48 channels) for inverse assembly. The analysis probe contains three additional pods for timing analysis.

Logic Analyzers Supported

Logic Analyzer	Channel Count	State Speed	Timing Speed	Memory Depth
16600A	204	100 MHz	125 MHz	64 k states
16601A	136	100 MHz	125 MHz	64 k states
16602A	102	100 MHz	125 MHz	64 k states
16603A	68	100 MHz	125 MHz	64 k states
16550A (one card)	102/card	100 MHz	250 MHz	4 k states
16554A (one card)	68/card	70 MHz	125 MHz	512 k states
16555A (one card)	68/card	110 MHz	250 MHz	1 M states
16555D (one card)	68/card	110 MHz	250 MHz	2 M states
16556A (one card)	68/card	100 MHz	200 MHz	1 M states
16556D (one card)	68/card	100 MHz	200 MHz	2 M states
1660A/AS/C/CS/CP	136	100 MHz	250 MHz	4 k states
1661A/AS/C/CS/CP	102	100 MHz	250 MHz	4 k states
1662A/AS/C/CS/CP	68	100 MHz	250 MHz	4 k states
1670A	136	70 MHz	125 MHz	64 k or .5 M states
1670D	136	100 MHz	125 MHz	64 k or 1 M states
1671A	102	70 MHz	125 MHz	64 k or .5 M
1671D	102	100 MHz	125 MHz	64 k or 1 M
1672A	68	70 MHz	125 MHz	64 k or .5 M
1672D	68	100 MHz	125 MHz	64 k or 1 M

Logic analyzer software version requirements

The logic analyzers must have software with a version number greater than or equal to those listed below to make a measurement with the HP E2415B. You can obtain the latest software at the following web site:

www.hp.com/go/logicanalyzer

If your software version is older than those listed, load new system software with the above version numbers or higher before loading the HP E2415B software.

Logic Analyzer Software Version Requirements

Logic Analyzer	Minimum Logic Analyzer Software Version for use with HP E2415B
HP 16600 Series	The latest HP 16600 logic analyzer software version is on the CD-ROM shipped with this product.
HP 1660A/AS Series	A.03.01
HP 1660C/CS/CP Series	A.02.01
HP 1670A/D Series	A.02.01
Mainframes*	
HP 16700 Series	The latest HP 16700 logic analyzer software version is on the CD-ROM shipped with this product.
HP 16500C Mainframe	A.01.05
HP 16500B Mainframe	A.03.14

* The mainframes are used with the HP 16550 and HP 16554/55/56 logic analyzer modules.

Equipment Used with the Analysis Probe

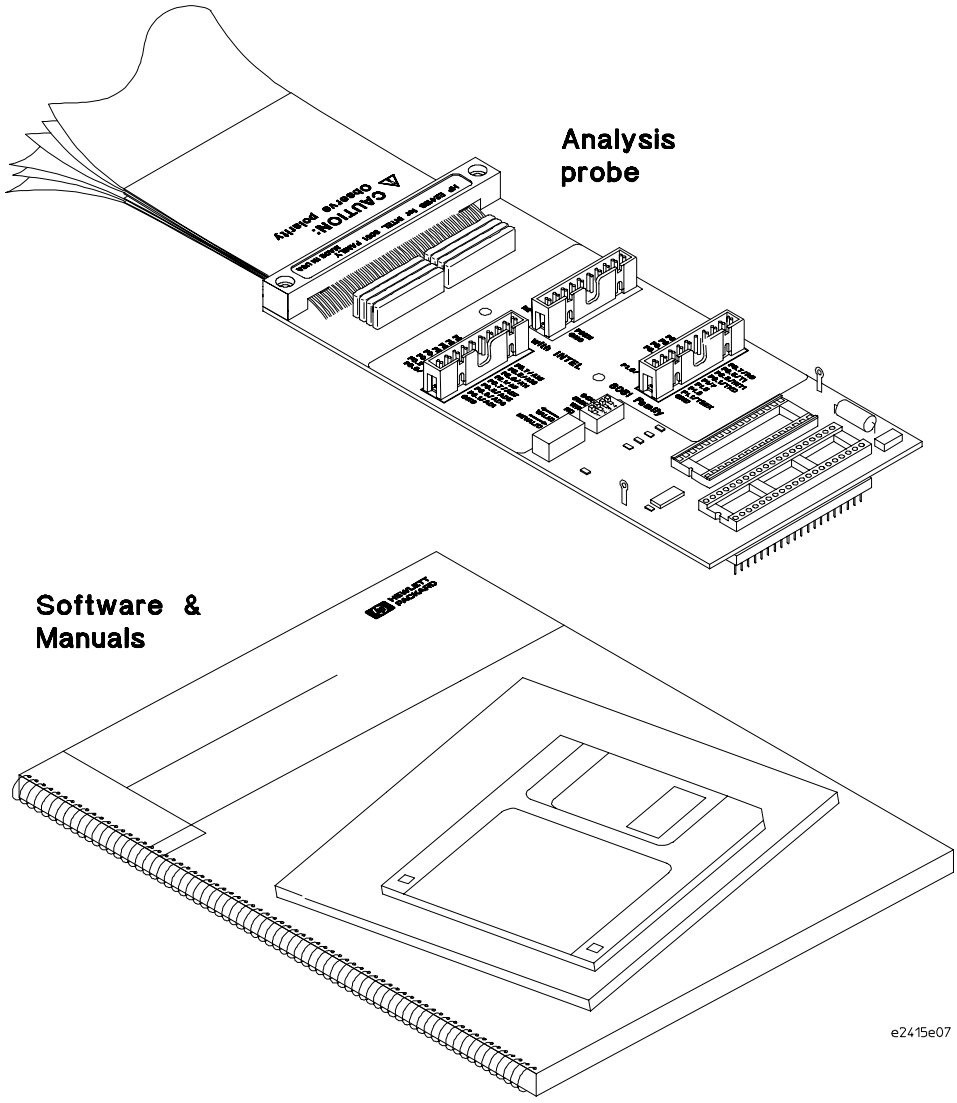
This section lists equipment used with the analysis probe. This information is organized under the following titles:

- Equipment supplied
- Minimum equipment required
- Additional equipment supported

Equipment supplied

The equipment supplied with the analysis probe is shown in the illustration on the next page. It is listed below:

- The analysis probe circuit card.
- Logic analyzer configuration files and inverse assembler software on a 3.5-inch disk.
- Logic analyzer configuration files and inverse assembler software on a CD-ROM.
- This User's Guide.



Equipment Supplied with the HP E2415B

Minimum equipment required

For state and timing analysis of an 8051-compatible target system, you need all of the following items.

- The HP E2415B Analysis Probe.
- For PLCC target systems, a PLCC-to-DIP adapter.
- For timing analysis, either 100 kOhm Termination Adapters (HP part number 01650-63203) or the General Purpose (GP) probes supplied with your logic analyzer. Three 16-channel connectors are provided on the analysis probe for timing analysis.
- One of the logic analyzers listed on page 1-4. The logic analyzer software version requirements are listed on page 1-5.

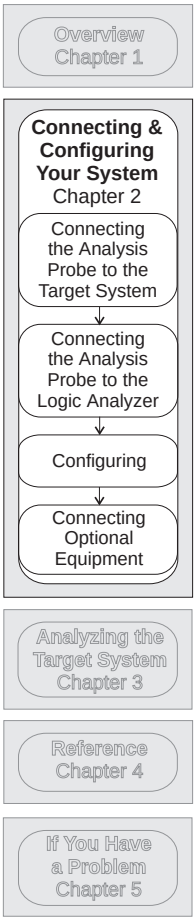
Additional equipment supported

The HP E2415B does not support any additional equipment.

2

Connecting and Configuring Your System

Connecting and Configuring Your System

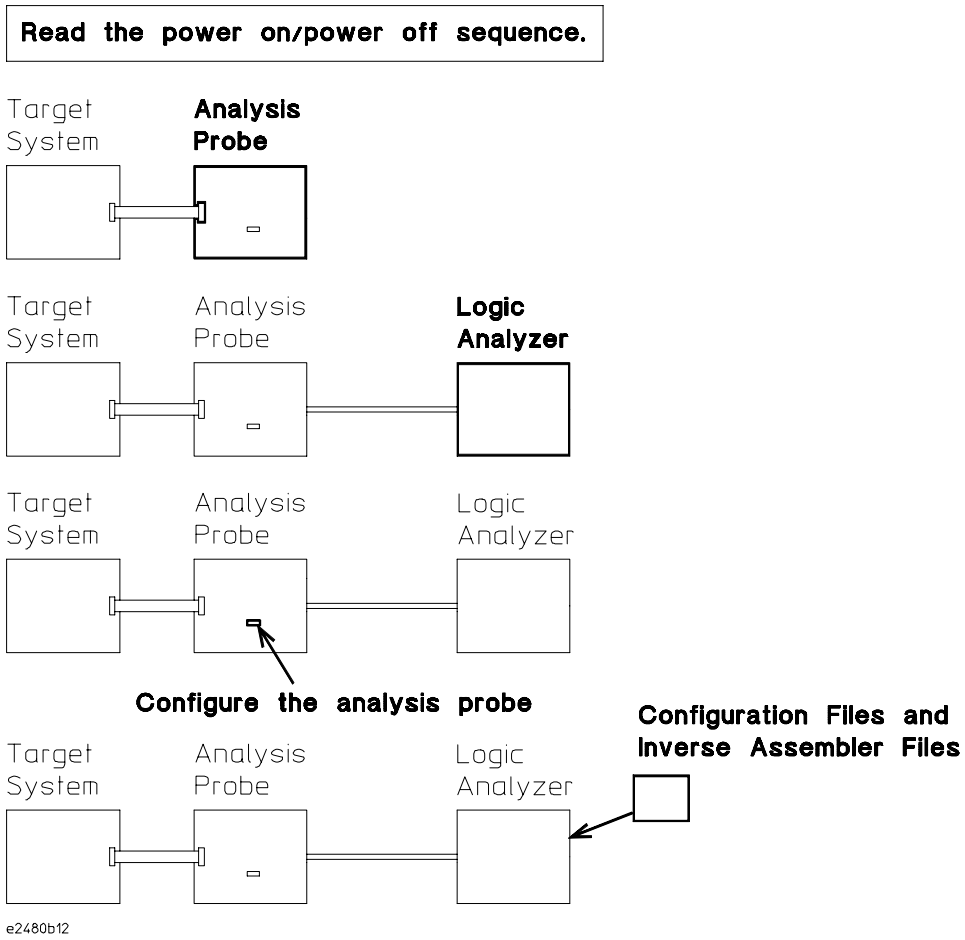


This chapter shows you how to connect the logic analyzer to the target system through the analysis probe.

If you are connecting to an HP 16600 Series or HP 16700 Series Logic Analyzer, follow the instructions given onscreen in the Setup Assistant for connecting and configuring your system. Use this manual for additional information, if desired. Refer to chapter 1 for a description of Setup Assistant.

If you are not using the Setup Assistant, follow the instructions given in this chapter. This chapter is divided into the following sections; the order shown here is the recommended order for performing these tasks:

- Read the power on/power off sequence
- Connect the analysis probe to the target system
- Connect the analysis probe to the logic analyzer
- Configure the analysis probe
- Configure the logic analyzer
- Connect optional equipment



Connection Sequence

Power-on/Power-off Sequence

Listed below are the sequences for powering on and off a fully connected system. Simply stated, your target system is always the last to be powered on, and the first to be powered off.

To power on HP 16600 and HP 16700 series logic analysis systems

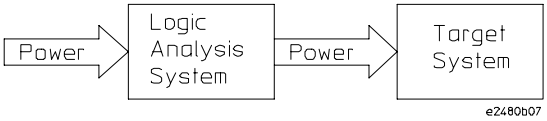
Ensure the target system is powered off.

1. Turn on the logic analyzer. The Setup Assistant will guide you through the process of connecting and configuring the analysis probe.
2. When the analysis probe is connected to the target system and logic analyzer, and everything is configured, turn on your target system.

To power on all other logic analyzers

With all components connected, power on your system in the following order:

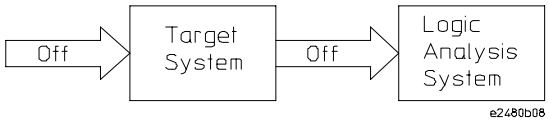
1. Logic analysis system.
2. Your target system.



To power off

Turn off power to your system in the following order:

1. Turn off your target system.
2. Turn off your logic analysis system.



Connecting the Analysis Probe to the Target System

Overview
Chapter 1
Connecting & Configuring Your System
Chapter 2
Connecting the Analysis Probe to the Target System
Connecting the Analysis Probe to the Logic Analyzer
Configuring
Connecting Optional Equipment
Analyzing the Target System
Chapter 3
Reference
Chapter 4
If You Have a Problem
Chapter 5

This section explains how to connect the HP E2415B Analysis Probe to the target system. For information on connecting the analysis probe to the target system, refer to the following sections:

- For DIP target systems, refer to "To connect to a DIP target system."
- For PLCC target systems, refer to "To connect to a PLCC target system."

Protect Your Equipment

The analysis probe socket assembly pins are covered for shipment with a conductive foam wafer or conductive plastic pin protector. This is done to protect the delicate gold-plated pins from damage due to impact. When you are not using the analysis probe, protect the socket assembly pins from damage by covering them with the pin protector.

To connect to a DIP target system

The microcontroller connector on the analysis probe will connect directly to a DIP microcontroller socket on the target system. To connect the microcontroller connector to the target system:

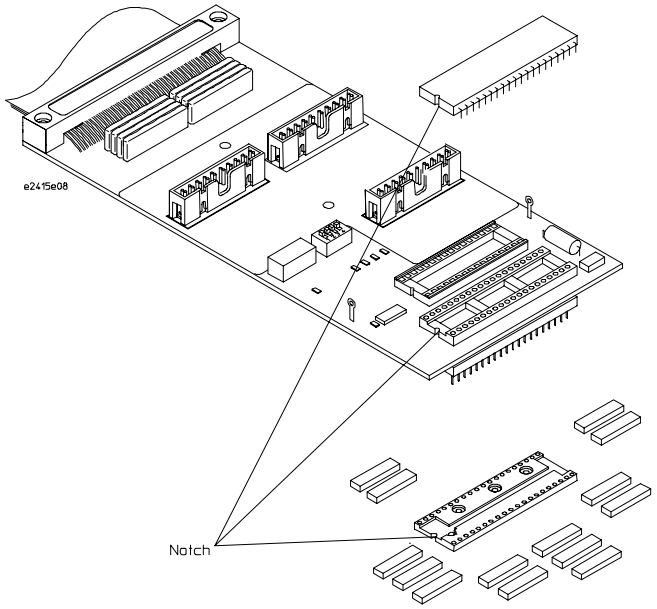
CAUTION

Equipment Damage. To prevent equipment damage, remove power from the target system and make sure no logic analyzer cables are connected to the analysis probe.

- Remove the microcontroller from the target system and install it in socket XU1 of the analysis probe.
- If the target system does not have a socket in the microcontroller position, install one.
- Attach the analysis probe to the microcontroller socket on the target system.

CAUTION

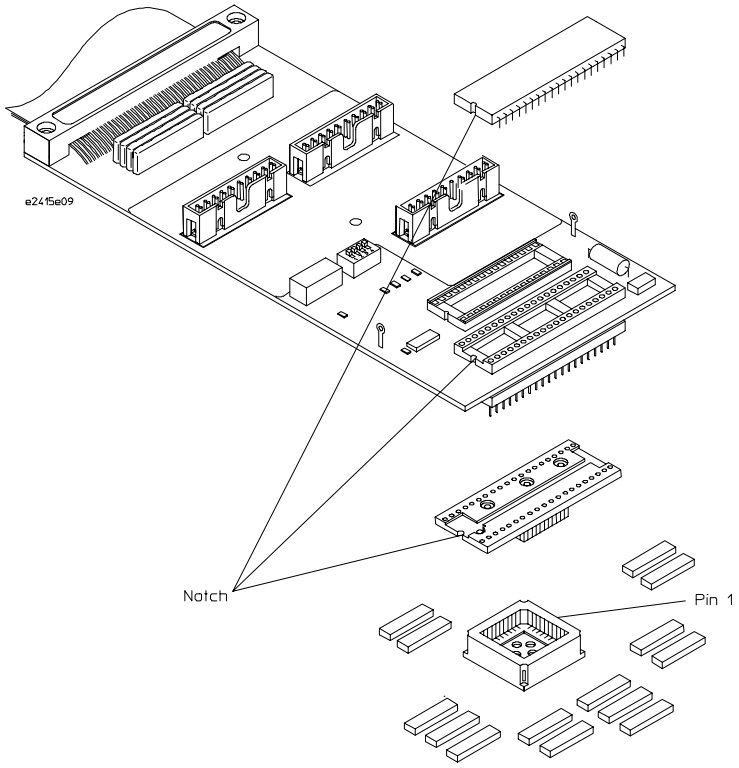
Care must be taken to align the notch of the cable assembly socket with the notch of the microcontroller socket on the target system to prevent mis-alignment or damage. The notch is shown on the illustration below.



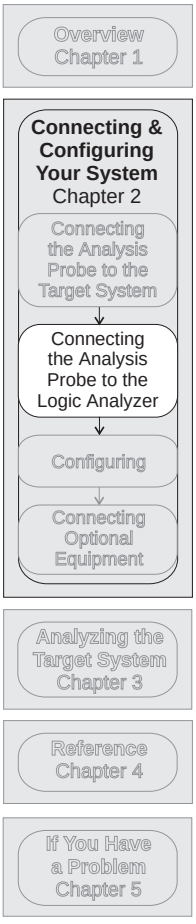
To connect to a PLCC target system

If the target system contains a PLCC microcontroller, a PLCC-to-DIP adapter must first be attached to the target system. Adapters are available from Emulation Technology. For soldered PLCC microcontrollers, use ET part number AC-DIP-PCC-8031/51. For socketed PLCC microcontrollers, use ET part number AS-DIP-PCC-8031/51. For socketed PLCC systems, a 40-pin DIP microcontroller equivalent to the PLCC must be installed into the analysis probe socket XU1.

Follow any instructions provided with the adapter to connect the adapter to the target system. The analysis probe then attaches to the adapter.



Connecting the Analysis Probe to the Logic Analyzer



The following sections show the connections between the logic analyzer pod cables and the analysis probe connectors. Use the appropriate section for your logic analyzer. The configuration file names for each logic analyzer are located at the bottom of the connection diagrams.

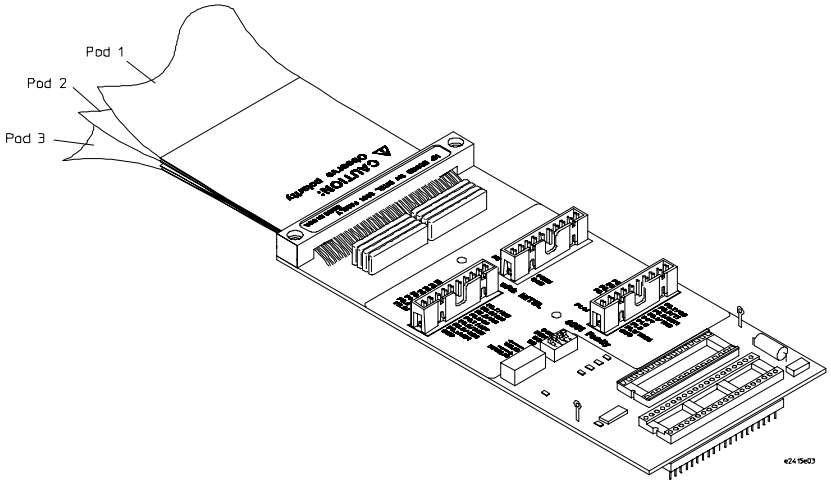
The figures on the following page show the State and Timing connectors. For State analysis, use State connectors P1, P2, and P3. For Timing analysis, use either General Purpose probes or termination adapters, and connect to Timing connectors P1, P2, and P3.

This section provides connection diagrams for connecting the analysis probe to the logic analyzers listed below:

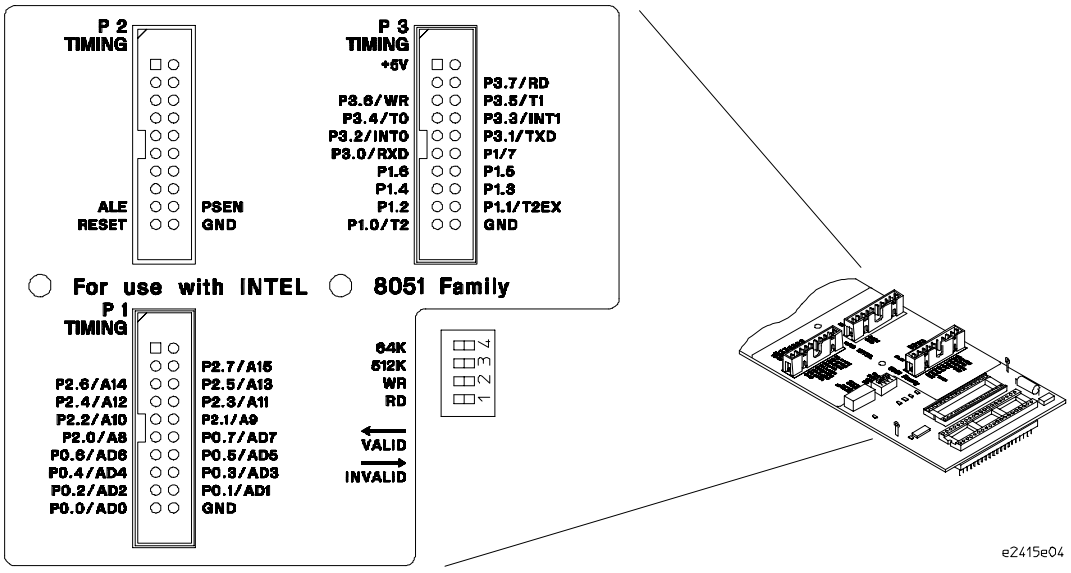
- HP 16600A logic analysis system
- HP 16601A logic analysis system
- HP 16602A logic analysis system
- HP 16603A logic analysis system
- HP 16550A logic analyzers (one card)
- HP 16554/55/56 logic analyzers (one card)
- HP 1660A/AS/C/CS/CP logic analyzers
- HP 1661A/AS/C/CS/CP logic analyzers
- HP 1662A/AS/C/CS/CP logic analyzers
- HP 1670A/D logic analyzers
- HP 1671A/D logic analyzers
- HP 1672A/D logic analyzers

Analysis probe pod locations

The illustrations below show the pod locations on the analysis probe.



Analysis Probe State Pod Numbers



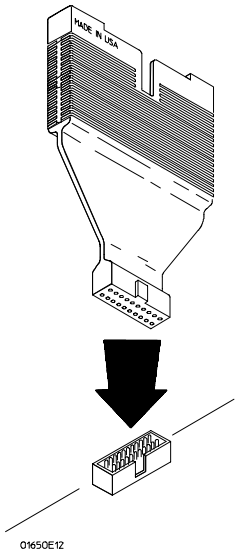
Analysis Probe Timing Pod Numbers

To connect the termination adapters

The nonterminated Timing connectors (Timing P1 to P3) must be probed by using either the General Purpose probes (shipped with the logic analyzer) or the 100 kOhm Termination Adapters (HP part number 01650-63203). The State connectors have built-in termination and do not require termination adapters.

To connect the termination adapters for Timing analysis:

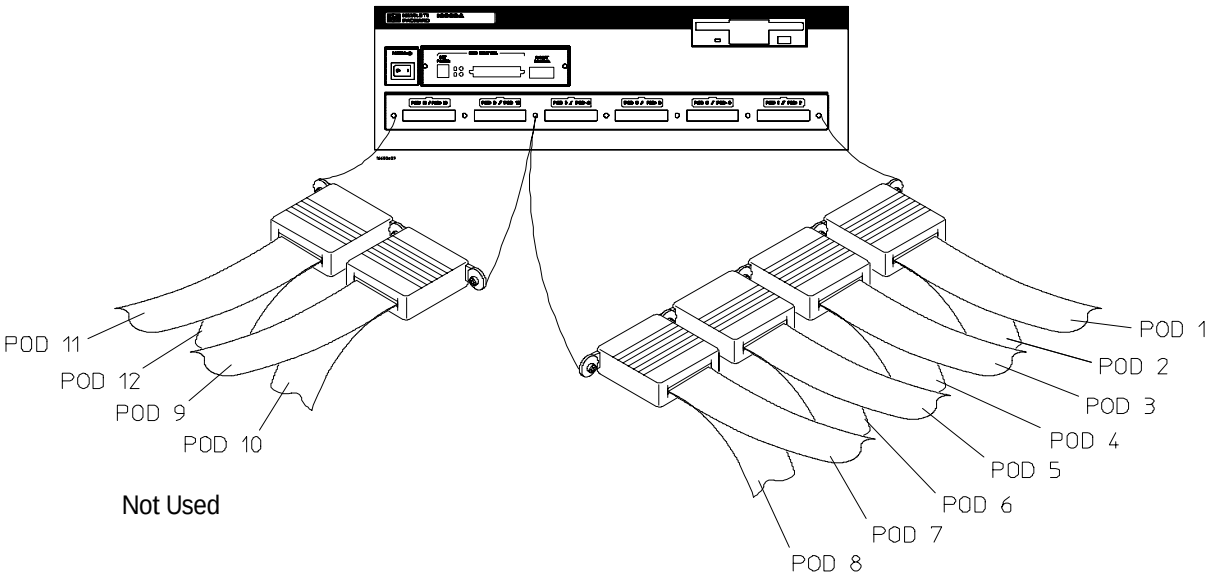
- Align the key on the male end of the termination adapter with the slot on the connector of one of the logic analyzer cables. Push the termination adapter into the connector.
- Connect the female end of the termination adapter to the analysis probe.



Connecting the Termination Adapters for Timing Analysis

To connect to the HP 16600A logic analyzer

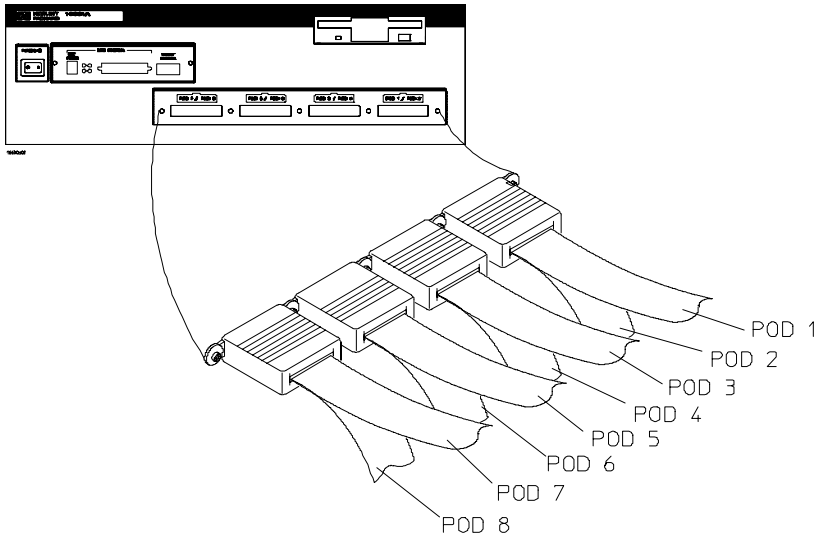
Use the figure and table below to connect the analysis probe to the HP 16600A logic analyzer. For State analysis, connect the logic analyzer to the State pods P1, P2, and P3. For Timing analysis, connect the logic analyzer to the Timing pods P1, P2, and P3 (see page 2-9).



Logic Analyzer Pod HP 16600A	Configuration File (State)	Configuration File (Timing)	Pod 3	Pod 2	Pod 1
HP E2415B Connector	F_8051_S	F_8051_T	P3 DATA Lclk↑	P2 STAT Kclk↑	P1 ADDR Jclk↑

To connect to the HP 16601A logic analyzer

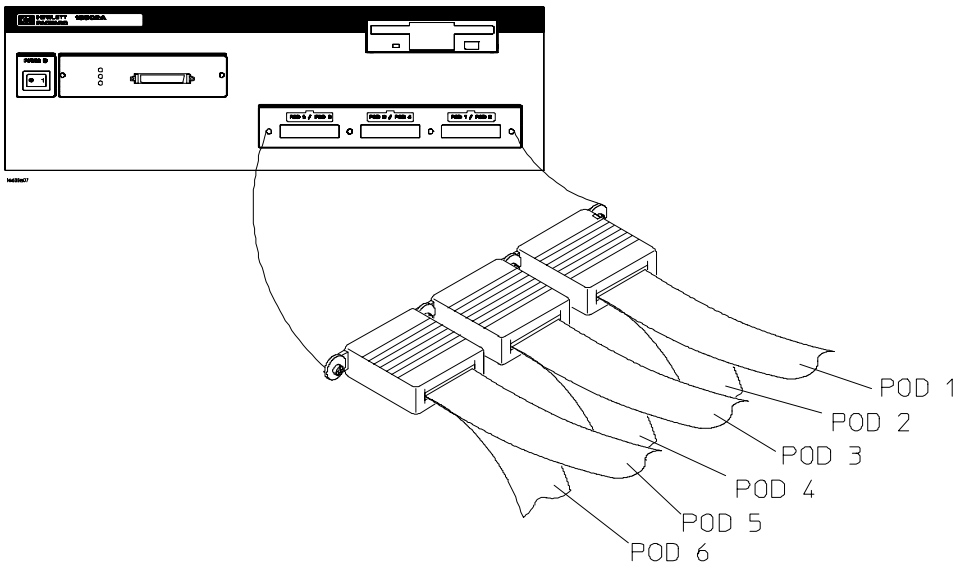
Use the figure and table below to connect the analysis probe to the HP 16601A logic analyzer. For State analysis, connect the logic analyzer to the State pods P1, P2, and P3. For Timing analysis, connect the logic analyzer to the Timing pods P1, P2, and P3 (see page 2-9).



Logic Analyzer Pods HP 16601A	Configuration File (State)	Configuration File (Timing)	Pod 3	Pod 2	Pod 1
HP E2415B Connector	F_8051_S	F_8051_T	P3 DATA Lclk↑	P2 STAT Kclk↑	P1 ADDR Jclk↑

To connect to the HP 16602A logic analyzer

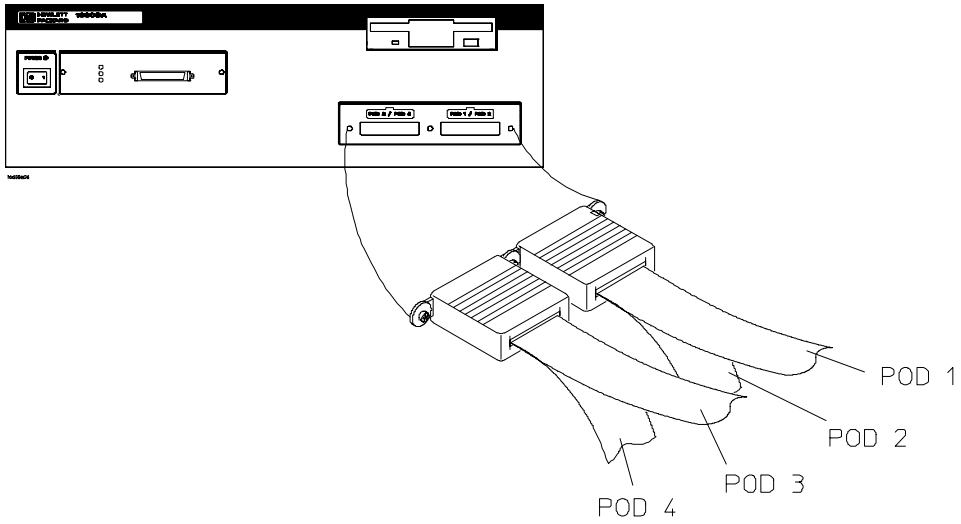
Use the figure and table below to connect the analysis probe to the HP 16602A logic analyzer. For State analysis, connect the logic analyzer to the State pods P1, P2, and P3. For Timing analysis, connect the logic analyzer to the Timing pods P1, P2, and P3 (see page 2-9).



Logic Analyzer Pods HP 16602A	Configuration File (State)	Configuration File (Timing)	Pod 3	Pod 2	Pod 1
HP E2415B Connector	F_8051_S	F_8051_T	P3 DATA Lclk↑	P2 STAT Kclk↑	P1 ADDR Jclk↑

To connect to the HP 16603A logic analyzer

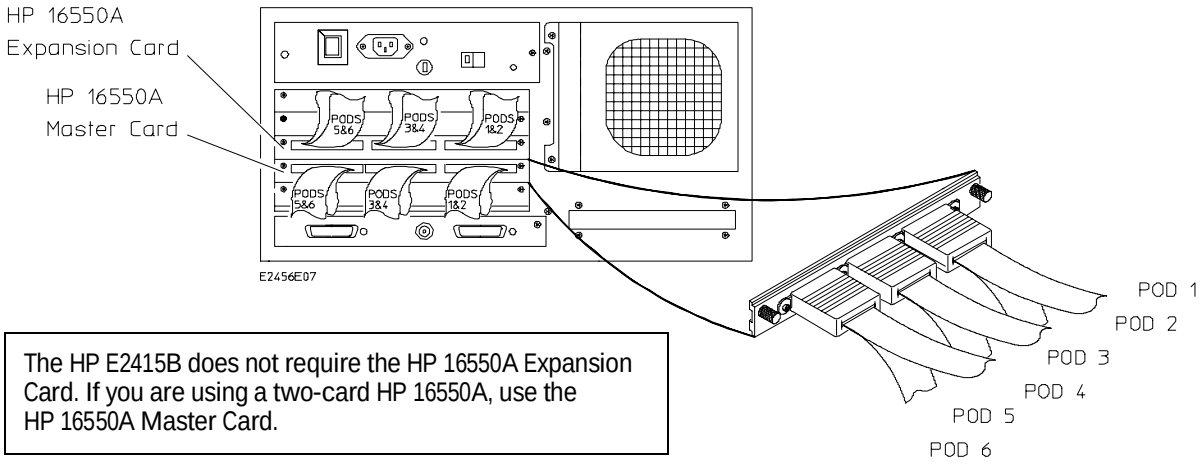
Use the figure and table below to connect the analysis probe to the HP 16603A logic analyzer. For State analysis, connect the logic analyzer to the State pods P1, P2, and P3. For Timing analysis, connect the logic analyzer to the Timing pods P1, P2, and P3 (see page 2-9).



Logic Analyzer Pods HP 16603A	Configuration File (State)	Configuration File (Timing)	Pod 3	Pod 2	Pod 1
HP E2415B Connector	F_8051_S	F_8051_T	P3 DATA Lclk↑	P2 STAT Kclk↑	P1 ADDR Jclk↑

To connect to the HP 16550A logic analyzer

Use the figure and table below to connect the analysis probe to the HP 16550A logic analyzer. For State analysis, connect the logic analyzer to the State pods P1, P2, and P3. For Timing analysis, connect the logic analyzer to the Timing pods P1, P2, and P3 (see page 2-9).

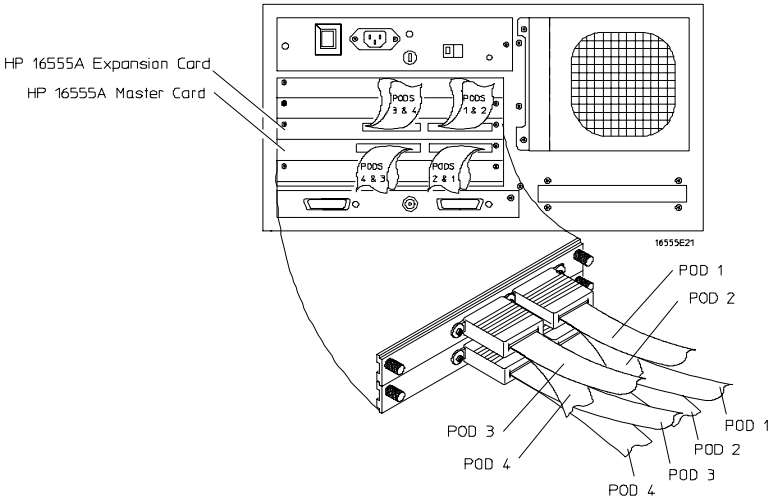


The HP E2415B does not require the HP 16550A Expansion Card. If you are using a two-card HP 16550A, use the HP 16550A Master Card.

Logic Analyzer Pods HP 16550A (use Master Card)	Configuration File (State)	Configuration File (Timing)	Pod 3	Pod 2	Pod 1
HP E2415B Connector	F_8051_S	F_8051_T	P3 DATA Lclk↑	P2 STAT Kclk↑	P1 ADDR Jclk↑

To connect to the HP 16554/55/56 logic analyzers

Use the figure and table below to connect the analysis probe to the HP 16554A/55A/56A and HP 16555D/56D logic analyzers. For State analysis, connect the logic analyzer to the State pods P1, P2, and P3. For Timing analysis, connect the logic analyzer to the Timing pods P1, P2, and P3 (see page 2-9).

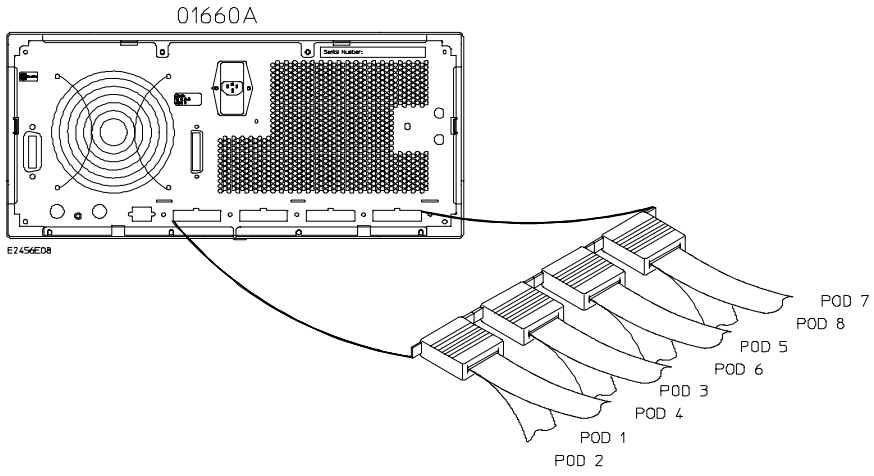


The HP E2415B analysis probe does not require the HP 16554/55/56 Expansion Cards. If you are using a multi-card HP 16554/55/56, use the HP 16554/55/56A Master Card.

Logic Analyzer Pods HP 16554/55/56 (use Master Card)	Configuration File (State)	Configuration File (Timing)	Pod 3	Pod 2	Pod 1
HP E2415B Connector	G_8051_S	G_8051_T	P3 DATA Lclk↑	P2 STAT Kclk↑	P1 ADDR Jclk↑

To connect to the HP 1660A/AS/C/CS/CP logic analyzers

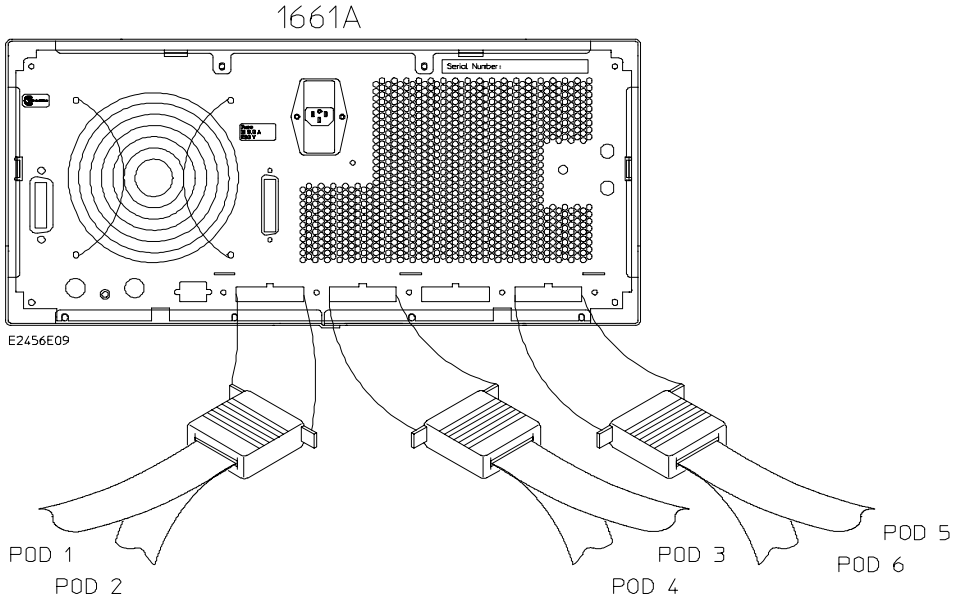
Use the figure and table below to connect the analysis probe to the HP 1660A/C logic analyzers. For State analysis, connect the logic analyzer to the State pods P1, P2, and P3. For Timing analysis, connect the logic analyzer to the Timing pods P1, P2, and P3 (see page 2-9).



Logic Analyzer Pods HP 1660 series	Configuration File (State)	Configuration File (Timing)	Pod 3	Pod 2	Pod 1
HP E2415B Connector	F_8051_S	F_8051_T	P3 DATA Lclk↑	P2 STAT Kclk↑	P1 ADDR Jclk↑

To connect to the HP 1661A/AS/C/CS/CP logic analyzers

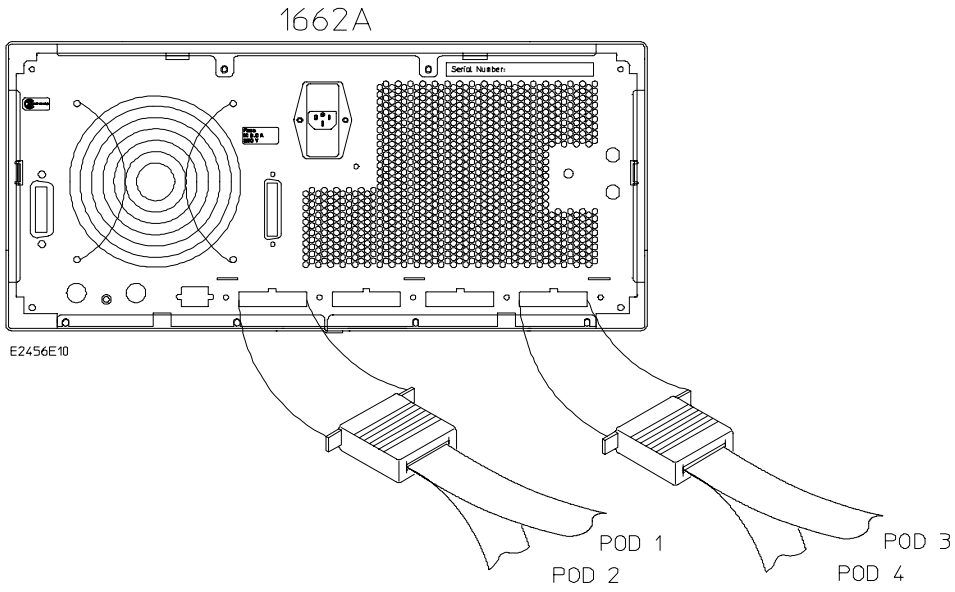
Use the figure and table below to connect the analysis probe to the HP 1661A/C logic analyzers. For State analysis, connect the logic analyzer to the State pods P1, P2, and P3. For Timing analysis, connect the logic analyzer to the Timing pods P1, P2, and P3 (see page 2-9).



Logic Analyzer Pods HP 1661 series	Configuration File (State)	Configuration File (Timing)	Pod 3	Pod 2	Pod 1
HP E2415B Connector	F_8051_S	F_8051_T	P3 DATA Lclk↑	P2 STAT Kclk↑	P1 ADDR Jclk↑

To connect to the HP 1662A/AS/C/CS/CP logic analyzers

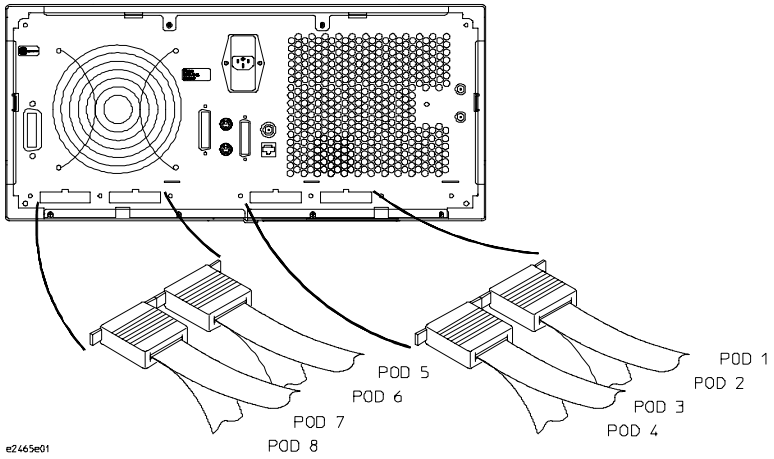
Use the figure and table below to connect the analysis probe to the HP 1662A/C logic analyzers. For State analysis, connect the logic analyzer to the State pods P1, P2, and P3. For Timing analysis, connect the logic analyzer to the Timing pods P1, P2, and P3 (see page 2-9).



Logic Analyzer Pods HP 1662 series	Configuration File (State)	Configuration File (Timing)	Pod 3	Pod 2	Pod 1
HP E2415B Connector	F_8051_S	F_8051_T	P3 DATA Lclk↑	P2 STAT Kclk↑	P1 ADDR Jclk↑

To connect to the HP 1670A/D logic analyzer

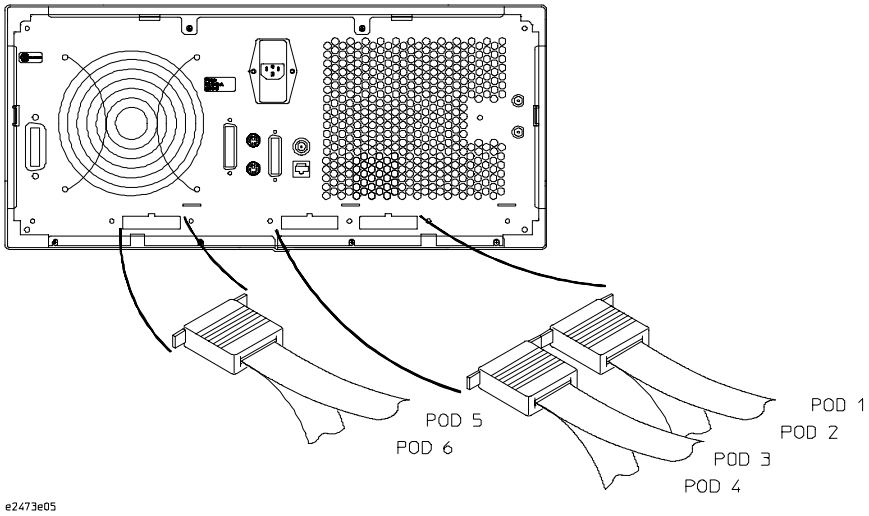
Use the figure and table below to connect the analysis probe to the HP 1670A/D logic analyzers. For State analysis, connect the logic analyzer to the State pods P1, P2, and P3. For Timing analysis, connect the logic analyzer to the Timing pods P1, P2, and P3 (see page 2-9).



Logic Analyzer Pods HP 1670 series	Configuration File (State)	Configuration File (Timing)	Pod 3	Pod 2	Pod 1
HP E2415B Connector	G_8051_S	G_8051_T	P3 DATA Lclk↑	P2 STAT Kclk↑	P1 ADDR Jclk↑

To connect to the HP 1671A/D logic analyzer

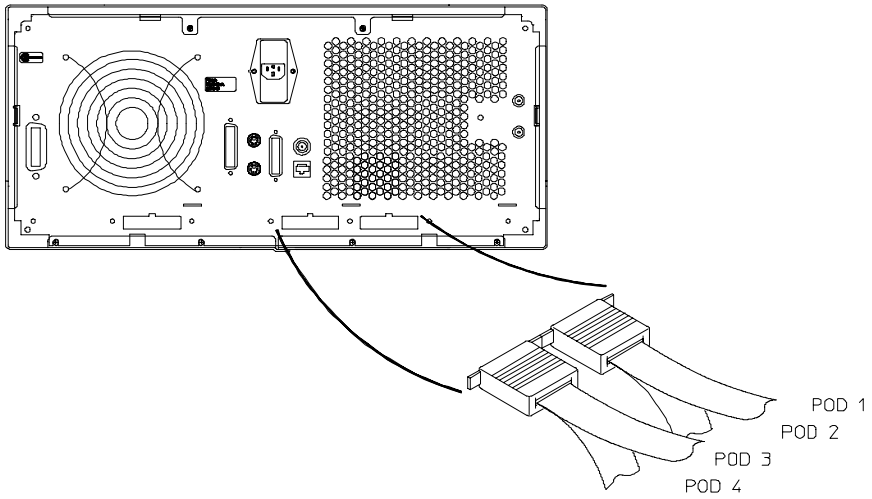
Use the figure and table below to connect the analysis probe to the HP 1671A/D logic analyzer. For State analysis, connect the logic analyzer to the State pods P1, P2, and P3. For Timing analysis, connect the logic analyzer to the Timing pods P1, P2, and P3 (see page 2-9).



Logic Analyzer Pods HP 1671 series	Configuration File (State)	Configuration File (Timing)	Pod 3	Pod 2	Pod 1
HP E2415B Connector	G_8051_S	G_8051_T	P3 DATA Lclk↑	P2 STAT Kclk↑	P1 ADDR Jclk↑

To connect to the HP 1672A/D logic analyzer

Use the figure and table below to connect the analysis probe to the HP 1672A/D logic analyzer. For State analysis, connect the logic analyzer to the State pods P1, P2, and P3. For Timing analysis, connect the logic analyzer to the Timing pods P1, P2, and P3 (see page 2-9).

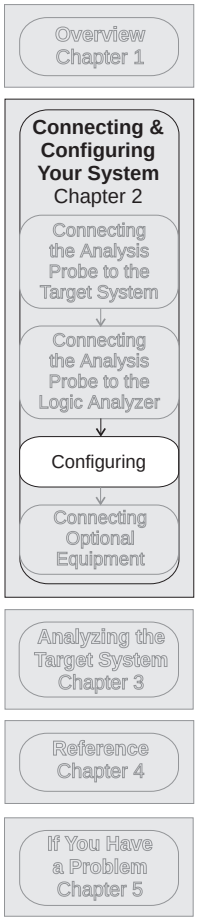


Logic Analyzer Pods HP 1672 series	Configuration File (State)	Configuration File (Timing)	Pod 3	Pod 2	Pod 1
HP E2415B Connector	G_8051_S	G_8051_T	P3 DATA Lclk↑	P2 STAT Kclk↑	P1 ADDR Jclk↑

Configuring

This section shows you how to configure the HP E2415B Analysis Probe and the logic analyzer. It consists of the following tasks:

- Configuring the analysis probe
- Configuring the logic analyzer



Configuring the Analysis Probe

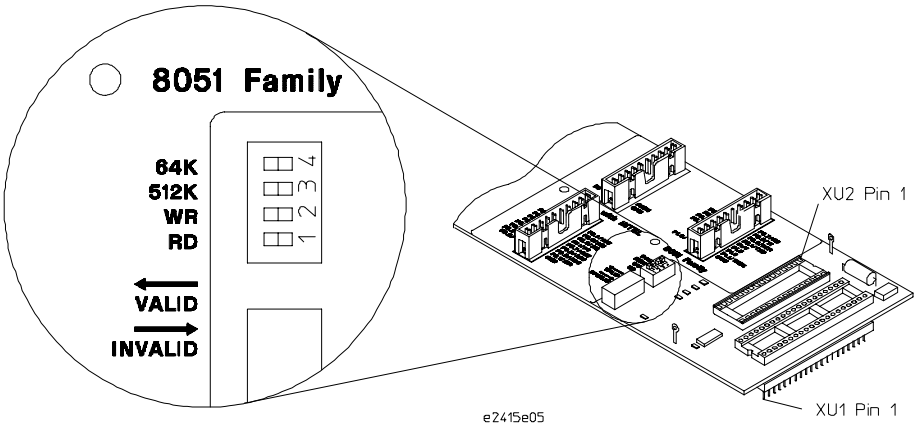
Configuring the analysis probe consists of the following:

- Configuring the analysis probe for RD and/or WR
- Connecting and configuring an external memory device

The RD/WR and external memory switches, and the external memory socket are shown below.

To configure the analysis probe for RD and/or WR

If the microcontroller is configured to use RD and/or WR signals from the target system, the analysis probe must also be configured for these signals. Set the RD and WR switches to VALID or INVALID according to the target system design (see figure below).



To connect and configure an external memory device

The HP E2415B provides a socket for installing a programmable memory device. This socket allows the user to map internal program memory to external, to aid in software debugging. The 32-pin socket will accept a 64k, 128k, 256k, or 512k memory device. The size of the memory device used in the analysis probe does not have to match the size used in the target system.

To connect and configure an external memory device:

- Program the memory device.
- Install the memory device into socket XU2, noting the location of pin 1 (see figure on previous page).
- Tie EA of the target system microcontroller to Vss (ground).
- Set the 64k and 512k switches according to the table below, to match the memory size of the device installed in the analysis probe.

Programmable Memory Switch Settings

Device Memory Size	64k Switch Setting	512k Switch Setting
64k	VALID	INVALID
128k	INVALID	INVALID
256k	INVALID	INVALID
512k	INVALID	VALID

Configuring the Logic Analysis System

You configure the logic analyzer by loading a configuration file. The information in the configuration file includes:

- Label names and channel assignments for the logic analyzer
- Inverse assembler file name

The configuration file you use is determined by the logic analyzer you are using. The configuration file names are listed with the logic analyzer connection tables, and in a table at the end of this section.

The procedures for loading a configuration file depend on the type of logic analyzer you are using. There is one procedure for the HP 16600/700 series logic analysis systems, and another procedure for the HP 1660-series, HP 1670-series, and logic analyzer modules in an HP 16500B/C mainframe. Use the appropriate procedures for your analyzer.

To load configuration and inverse assembler files — HP 16600/700 logic analysis systems

If you did not use Setup Assistant, you can load the configuration and inverse assembler files from the logic analysis system hard disk.

1 Click on the File Manager icon. Use File Manager to ensure that the subdirectory /hplogic/configs/hp/i8051/ exists.

> If the above directory does not exist, you need to install the I8051 Processor Support Package. Close File Manager, then use the procedure on the CD-ROM jacket to install the I8051 Processor Support Package before you continue.

2 Using File Manager, select the configuration file you want to load in the /hplogic/configs/hp/i8051/ directory, then click Load. If you have more than one logic analyzer installed in your logic analysis system, use the Target field to select the machine you want to load.

The logic analyzer is configured for 8051 analysis by loading the appropriate configuration file. Loading a state configuration file automatically loads the IA_8051E inverse assembler file.

3 If the target system microcontroller is compatible with an 8044, 8052, or 80251, the appropriate inverse assembler (IA_8044E, IA_8052E, or IA_80251E) should be used. To load a different inverse assembler, use File Manager, select the inverse assembler you want to load in the /hplogic/ia/ directory, then click Load.

4 Close File Manager.

To load configuration and inverse assembler files — other logic analyzers

If you have an HP 1660-series, HP 1670-series, or logic analyzer modules in an HP 16500B/C mainframe use these procedures to load the configuration file and inverse assembler.

The first time you set up the analysis probe, make a duplicate copy of the master disk. For information on duplicating disks, refer to the reference manual for your logic analyzer.

For logic analyzers that have a hard disk, you might want to create a directory such as 8051 on the hard drive and copy the contents of the floppy onto the hard drive. You can then use the hard drive for loading files.

1. **Insert the floppy disk in the front disk drive of the logic analyzer.**
2. **Go to the Flexible Disk menu.**
3. **Configure the menu to load.**
4. **Use the knob to select the appropriate configuration file.**

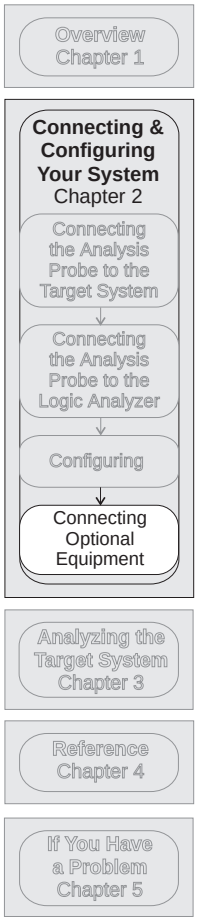
   Choosing the correct configuration file depends on which analyzer you are using. The configuration files are shown with the logic analyzer connection tables, and are also in the table on the next page.
5. **Select the appropriate analyzer on the menu. The HP 16500 logic analyzer modules are shown in the Logic Analyzer Configuration Files table.**
6. **Execute the load operation on the menu to load the file into the logic analyzer.**

   The logic analyzer is configured for 8051 analysis by loading the appropriate configuration file. Loading a state configuration file automatically loads the IA_8051E inverse assembler file. If the target system microcontroller is compatible with an 8044, 8052, or 80251, the appropriate inverse assembler (IA_8044E, IA_8052E, or IA_80251E) should be used. To load a different inverse assembler, repeat step 4 above, except this time select the desired inverse assembler.

Logic Analyzer Configuration Files

Analyzer Model	Analyzer Description (modules only)	Configuration File (State)	Configuration File (Timing)
16600A		F_8051_S	F_8051_T
16601A		F_8051_S	F_8051_T
16602A		F_8051_S	F_8051_T
16603A		F_8051_S	F_8051_T
16550A	100 MHz STATE 500 MHz TIMING	F_8051_S	F_8051_T
16554A	0.5M SAMPLE 70/125 MHz LA	G_8051_S	G_8051_T
16555A	1.0M SAMPLE 110/250 MHz LA	G_8051_S	G_8051_T
16555D	2.0M SAMPLE 110/250 MHz LA	G_8051_S	G_8051_T
16556A	1.0M SAMPLE 100/200 MHz LA	G_8051_S	G_8051_T
16556D	2.0M SAMPLE 100/200 MHz LA	G_8051_S	G_8051_T
1660A/AS/C/CS		F_8051_S	F_8051_T
1661A/AS/C/CS		F_8051_S	F_8051_T
1662A/AS/C/CS		F_8051_S	F_8051_T
1670A/D		G_8051_S	G_8051_T
1671A/D		G_8051_S	G_8051_T
1672A/D		G_8051_S	G_8051_T

The HP E2415B does not support any additional equipment.

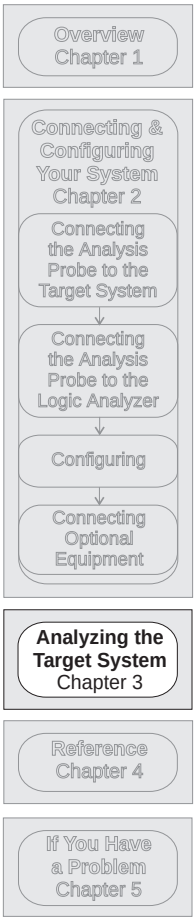


3

Analyzing the Target System

Analyzing the Target System

This chapter describes modes of operation for the HP E2415B Analysis Probe. It also describes analysis probe data, symbol encodings, and information about the inverse assemblers.



The information in this chapter is presented in the following sections:

- Modes of operation
- Logic analyzer configuration
- Using the inverse assemblers

Modes of Operation

The HP E2415B Analysis Probe can be used in two different analysis modes: State-per-transfer, and Timing. The following sections describe these operating modes and how to configure the logic analyzer for each mode.

State-per-transfer mode

In State-per-transfer mode, the analysis probe generates an acquisition clock only when there is a valid data transfer. This allows the logic analyzer to capture only valid data when it appears on the bus. The inverse assembler reconstructs the 8051 mnemonic from the hexadecimal data form.

Use the State configuration files to configure the logic analyzer for State-per-transfer mode.

Timing mode

In Timing mode, the latches on the analysis probe act like flow-through buffers. The signals from the microprocessor go directly from the target system to the logic analyzer, with a 1-ns channel-to-channel skew.

The Timing configuration files only provide labels for the Intel 8051-defined signals. If the target system has additional or different definitions, the Format menu should be modified appropriately and stored as a new Timing configuration.

Logic Analyzer Configuration

The following sections describe the logic analyzer configuration as set up by the configuration files.

Trigger specification

The trigger specification is set up by the software to store all states. If you modify the trigger specification to store only selected bus cycles, incorrect or incomplete inverse assembly may result.

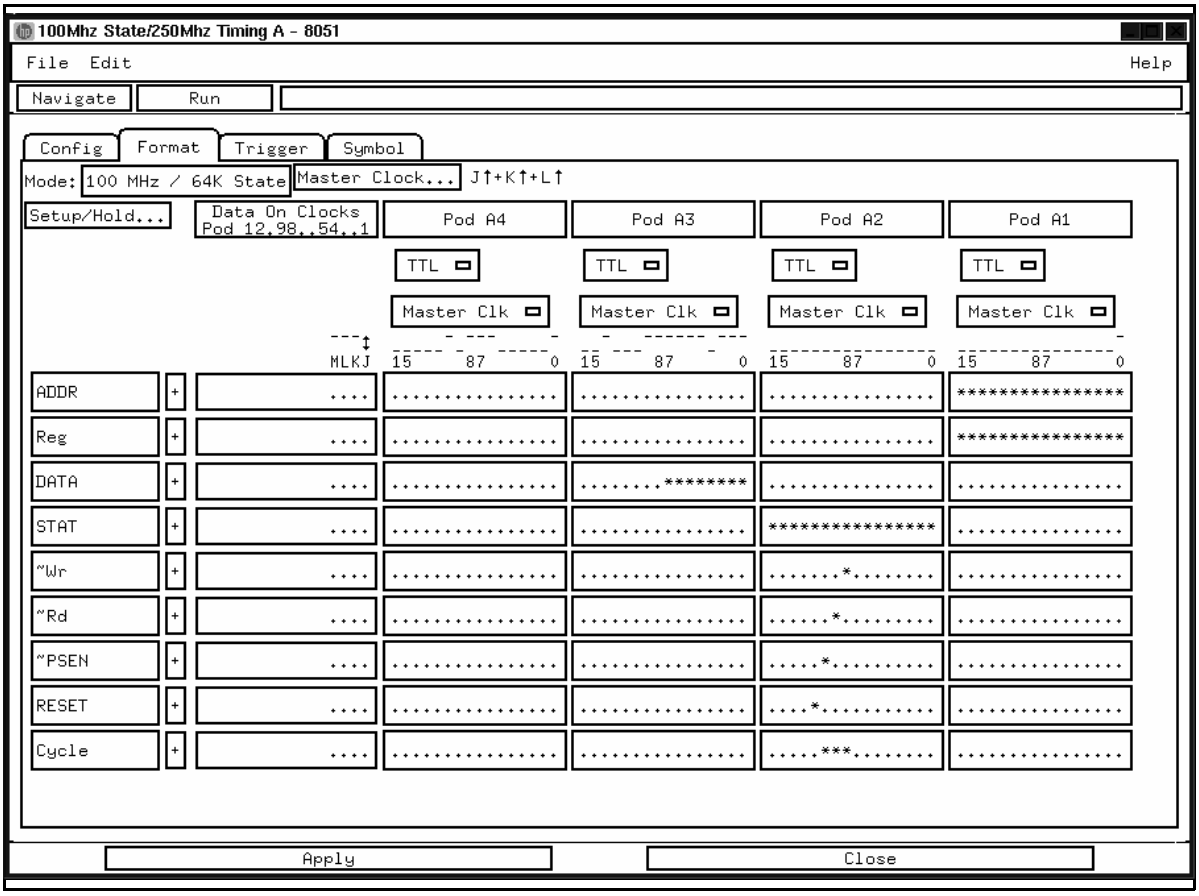
Format specification

When you use the HP E2415B analysis probe, the format specification set up by the software will be similar to the that shown on the following page. There may be some slight differences in the displays depending on which logic analyzer you are using.

The Timing configuration files only provide labels for the Intel 8051-defined signals. If the target system has additional or different definitions, the Format menu should be modified appropriately and stored as a new Timing configuration.

The tables in chapter 4 list the microcontroller signals for the HP E2415B analysis probe and their corresponding lines to the logic analyzer.

Do not modify the ADDR, DATA, or STAT labels in the state format specification if you want inverse assembly. Changes may cause incorrect results.



State Format Specification

Status Encoding

Each of the bits of the STAT label is described in the table below.

Status Bits

Bit	Status Signals	Description
0	WR	This signal is low for data write cycles.
1	RD	This signal is low for a data read cycle.
2	PSEN	This signal is low for a program fetch or interrupt.
3	RESET	This signal is high for RESET.

Logic Analyzer Symbols

The HP E2415B configuration software sets up symbol tables on the logic analyzer. The tables contain alphanumeric symbols which identify data patterns or ranges. Labels have been defined in the format specification menu to make triggering on specific cycles easier. The label base in the symbols menu is set to hexadecimal to conserve space in the listing menu.

The following table lists the symbols displayed in the Cycle field of the Listing menu.

Cycle Symbols

Symbol	Pattern
Mem Wr	0 1 1 0
Mem Rd	0 1 0 1
Prg Rd	0 0 1 1
RESET	1 x x x

Due to the large number of 8051 derivatives, the symbol definitions for the SFR memory map (loaded with the state configuration file) conform to the Intel 8051. If additional registers are defined for a specific 8051 derivative, you may add these registers to the symbol table of the configuration file and store this new configuration file with a different name.

Using the Inverse Assemblers

This section discusses the general output format of the inverse assemblers. It assumes that an inverse assembler has been loaded.

To select the appropriate inverse assembler

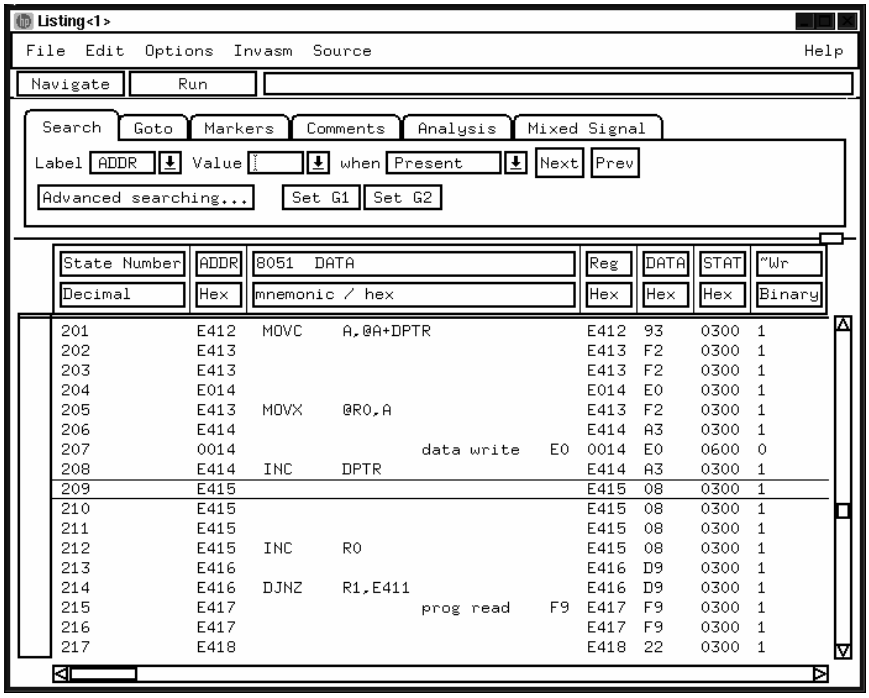
If the target system microcontroller is compatible with an 8044, 8052, or 80251, the IA_8044_E, IA_8044_E, or IA_80251_E inverse assembler should be used. All other microcontrollers use the IA_8051_E inverse assembler, which is loaded by default. The inverse assemblers are designed to display the appropriate symbolic name for all defined registers in the SFR memory range of the given microcontroller.

To load a different inverse assembler, use the procedure in chapter 2.

To display captured state data

The logic analyzer displays captured data in the Listing menu. The inverse assembler disassembles the captured data in a format that closely resembles the assembly source code for your processor.

If your trace listing doesn't otherwise appear to be correct (capturing the same RAM address twice, for example), make sure the analysis probe hardware is configured for state analysis. The "Invasm" field will appear at the top of the Listing menu screen when the logic analyzer is configured for state analysis. See Chapter 2 to review the hardware configuration, correct it if needed, and then run the trace again.



Listing Menu

General output format

The next few paragraphs describe the general output format of the inverse assemblers.

Numeric Format

Unless a value is followed by a suffix character, numeric output from the inverse assemblers is in hexadecimal format. Decimal values will have a period (.) as the suffix character; binary values have a percent sign (%).

Missing Operands

An asterisk (*) in the inverse assembler output indicate a missing operand. Since the 8051 architecture does not support prefetching, missing operands should only occur at the end of the acquisition where the opcode was acquired but its operand(s) was not.

Unexecuted Fetches

State listings will frequently display states with no mnemonic text. These are states in which the microcontroller continues to assert PSEN while it is executing the instruction. Because the microcontroller ignores these "fetches," no mnemonic text is generated for them.

SFR Registers

The inverse assemblers are designed to display the appropriate symbolic name for all defined registers in the SFR memory range of the given microcontroller.

To align the inverse assembler

The 8051 microprocessor does not provide enough status information for the inverse assemblers to pick out the first word of an instruction fetch. To ensure correct disassembly, you may need to point to the first state of an instruction fetch. Once aligned, the inverse assembler will disassemble from this state through the end of the screen.

Use the following procedure to align the inverse assembler:

1. Select a line on the display that you know contains the first word of an instruction fetch.
2. Roll this line to the top of the display.

> Do not roll the instruction to the line number field at the left center screen. In the Listing Menu on page 3-8, line 201 is the top of the display.

3. Select the appropriate field for your analyzer.
   a. For the HP 16600/700 series analyzers, select "Invasm," then select "Align."
   b. For the other logic analyzers, select "Invasm Options" and use the "Code Synchronization" submenu.
4. Select "Align."

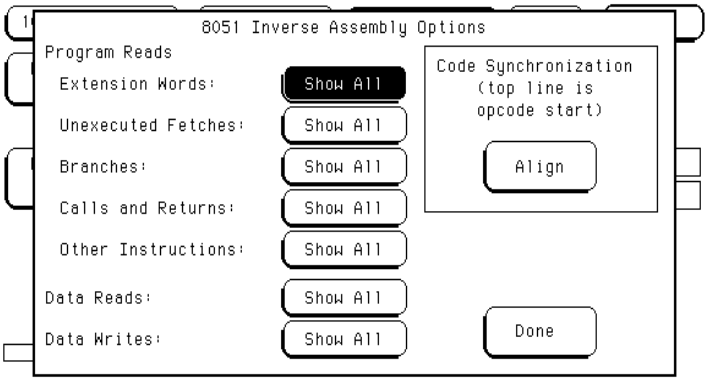
   The listing inverse assembles from the top line down. Any data before the top of the display is left unchanged.

   Rolling the display up inverse assembles the lines as they appear on the bottom of the display. If you jump to another area of the display by entering a new line number, you may need to re-align the inverse assembler by repeating steps 1 through 4.

   Each time you inverse assemble a block of memory, the analyzer will keep that block in the inverse assembled condition. You can inverse assemble several different blocks in the analyzer memory, but the activity between those blocks will not be inverse assembled.

To use the inverse assembly options

The Inverse Assembly Options menu contains two function: display filtering with Show/Suppress selections, and Code Synchronization (discussed in previous section). To access the Inverse Assembly Options menu, press the Invasm Options softkey at the top of the screen.



Inverse Assembly Options Menu

The Inverse Assembly Options menu is only available on the HP 1660-series, HP 1670-series, and HP 16500B/C mainframes.

Show/Suppress

The Show/Suppress settings determine whether certain classes of acquisition states are shown or suppressed on the logic analyzer display. The previous figure shows the microcontroller operations which have this option. The settings for the various operations do not affect the data which is stored by the logic analyzer, they only affect whether that data is displayed or not. The same data can be examined with different settings, for different analysis requirements.

This function allows faster analysis in two ways. First, unneeded information can be filtered out of the display. Second, particular operations can be isolated by suppressing all other operations. For example, I/O accesses can be shown, with all other operations suppressed, allowing quick analysis of I/O accesses.

If the X or O pattern markers are turned on, and the designated pattern is found in a state that has been Suppressed with display filtering, the following message will appear on the logic analyzer display: "X (or O) pattern found, but state is suppressed."

Code Synchronization

The Code Synchronization enables the inverse assembler to resynchronize with the microcontroller code (see previous section). If any of the Code Reads are suppressed, this could cause some executed instructions to be missing from the display. To resyncronize the inverse assembler, use the procedure described earlier.

Error messages

The following list of messages will help you identify operation errors.

Input Error This message indicates an error was encountered by the inverse assembler and that data acquired by the logic analyzer is not accessible. For example: An opcode fetch for an instruction that requires a second byte is found in the last location of the trace buffer.

Status Error Undefined opcode encountered. Microcontroller action cannot be determined.

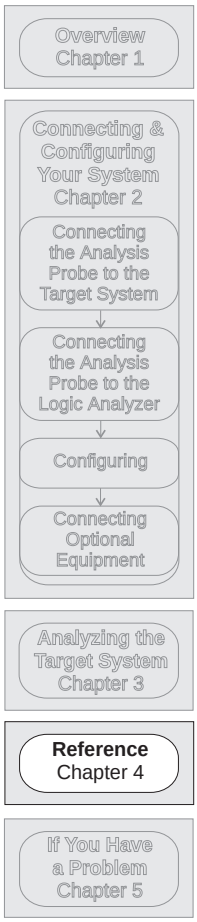
Reference

Reference

This chapter contains additional reference information including the signal mapping for the HP E2415B Analysis Probe.

The information in this chapter is presented in the following sections:

- Operating characteristics
- Theory of operation and clocking
- Signal-to-connector mapping
- Circuit board dimensions
- Replaceable parts



Operating characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the analysis probe.

Product Characteristics

Microcontrollers Supported	Intel MCS-51 and Intel RUPI-44, and all microcontrollers made by other manufacturers that comply with Intel MCS-51 and Intel RUPI-44 specifications.
Package Supported	40-pin dual-in-line (DIP) or 44-pin PLCC.
Accessories Required	PLCC-to-DIP adapter for probing 44-pin PLCC.
Logic Analyzer Required	HP 1660A/AS/C/CS/CP, HP 1661A/AS/C/CS/CP, HP 1662A/AS/C/CS/CP, HP 1670A/D, HP 1671A/D, HP 1672A/D, HP 16550A (one card), HP 16554A/55A/56A (one card), HP 16555D/56D (one card), HP 16600A, HP 16601A, HP 16602A, HP 16603A.
Number of Probes Used	Three 16-channel probes required for state analysis. Up to three probes required for timing analysis.
Microcontroller Operations Displayed	Data Read/Write Illegal opcodes Opcode/Operand Fetches
Additional Capabilities	The microcontroller must be addressing external memory and/or peripheral devices for the logic analyzer to inverse assemble the state information.

Electrical Characteristics

Power Requirements	Maximum of 1.0 A at + 5 Vdc supplied by analyzer. CAT I, Pollution degree 2.
Signal Line Loading	PSEN output - 3 LS TTL loads plus 40 pF. WR output - 2 LS TTL loads plus 40 pF. RD output - 2 LS TTL loads plus 40 pF. All other monitored lines are 1 LS TTL load and 40 pF.
Maximum Clock Speed	42 MHz clock input.

Environmental Characteristics	This product is intended for indoor use only.	
Temperature	Operating	0 to + 55 degrees C +32 to +131 degrees F
	Nonoperating	-40 to + 75 degrees C -40 to +167 degrees F
Altitude	Operating	4,600 m (15,000 feet)
	Nonoperating	15,3000 m (50,000 feet)
Humidity	Up to 90% noncondensing. Avoid sudden , extreme temperature changes which could cause condensation on the circuit board.	

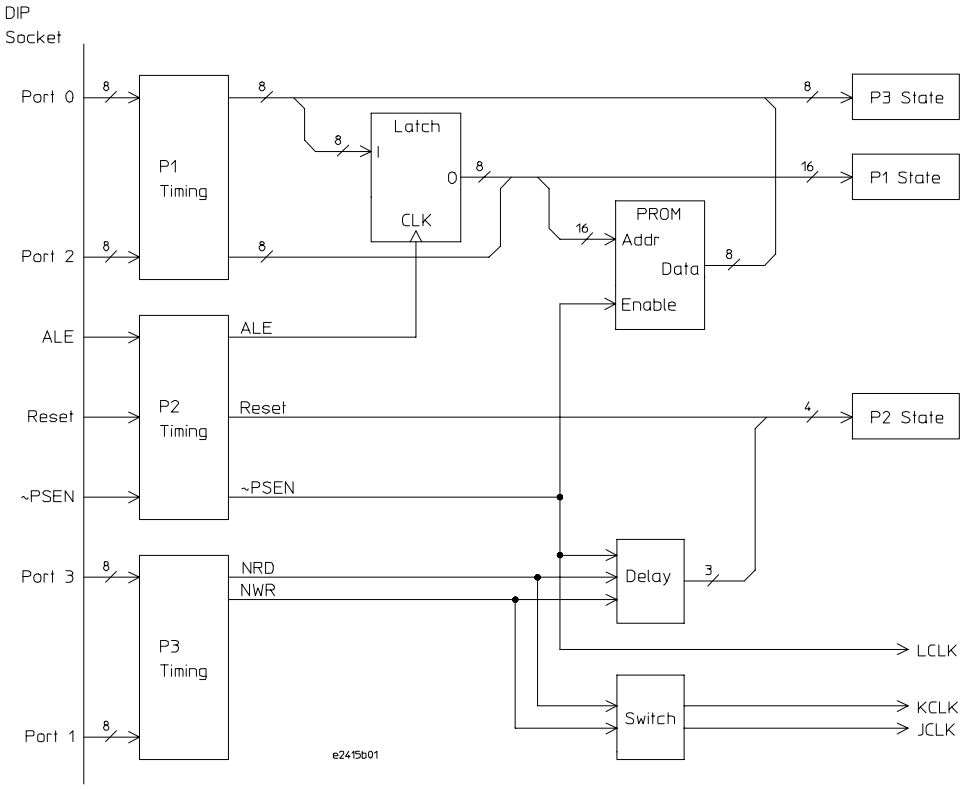
Theory of operation and clocking

The HP E2415B latches only the AD0 - AD7 signals to acquire A0 - A7. These signals are then available for capture by the logic analyzer and for generating an address for an on-board memory device.

The additional socket (XU2) allows the user to map any microcontroller Internal memory to External for software debug purposes. Memory devices from 64k to 512k can be used. The memory size switches correctly interface a memory device into the target system.

Since an 8051-compatible microcontroller executes only program reads, data reads, or data writes, the logic analyzer can be clocked by PSEN, RD, or WR. The RD/WR switches allow the user to disable RD and/or WR when used as generic I/O.

In order to obtain the proper status information, the signals PSEN, RD, and WR are delayed after clocking the logic analyzer to guarantee sufficient hold time. The figure on the following page shows a block diagram of the HP E2415B Analysis Probe.



HP E2415B Block Diagram

Microcontroller signal to HP E2415B connector mapping

The following tables describe the electrical interconnections implemented with the HP E2415B Analysis Probe. The first table shows the State connections, and the second table shows the Timing connections.

8051-compatible Signal List for State Connectors

PIN NAME	E2415B POD	ANALYZER PIN	LABEL
A0	P1	39	ADDR
A1	P1	37	ADDR
A2	P1	35	ADDR
A3	P1	33	ADDR
A4	P1	31	ADDR
A5	P1	29	ADDR
A6	P1	27	ADDR
A7	P1	25	ADDR
A8	P1	23	ADDR
A9	P1	21	ADDR
A10	P1	19	ADDR
A11	P1	17	ADDR
A12	P1	15	ADDR
A13	P1	13	ADDR
A14	P1	11	ADDR
A15	P1	9	ADDR
WR-	P1	3	clk

8051-compatible Signal List for State Connectors

PIN NAME	E2415B POD	ANALYZER PIN	LABEL
WR-	P2	23	STAT
RD-	P2	21	STAT
PSEN-	P2	19	STAT
RESET	P2	17	STAT
RD-	P2	3	clk
D0	P3	39	DATA
D1	P3	37	DATA
D2	P3	35	DATA
D3	P3	33	DATA
D4	P3	31	DATA
D5	P3	29	DATA
D6	P3	27	DATA
D7	P3	25	DATA
PSEN-	P3	3	clk

8051-compatible Signal List for Timing Connectors

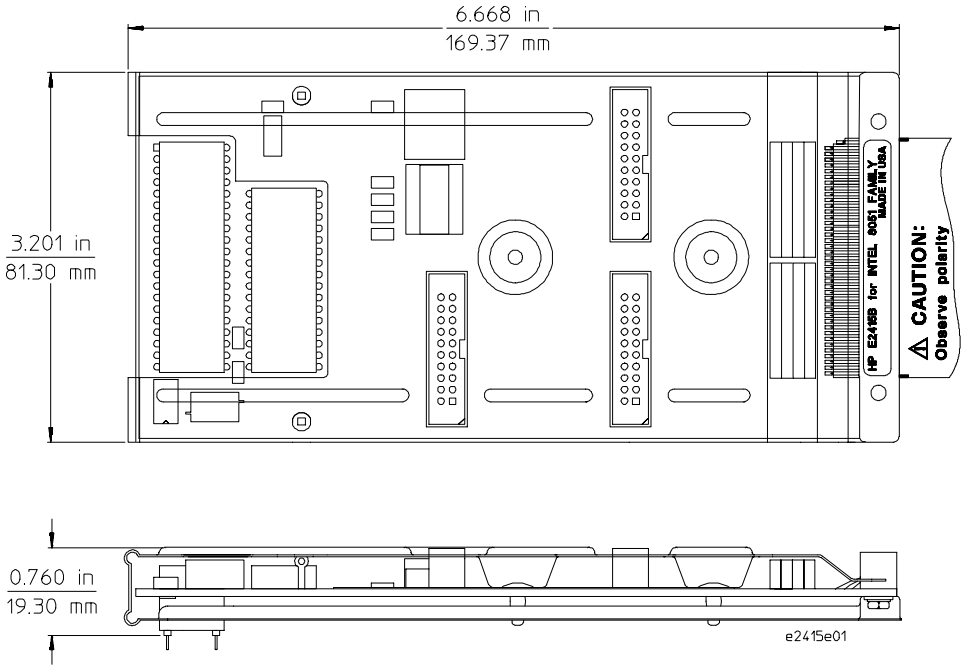
PIN NAME	E2415B POD	ANALYZER PIN	LABEL 1	LABEL 2	LABEL 3
P0_0	P0	19	Port 0	ADDR	DATA
P0_1	P1	18	Port 0	ADDR	DATA
P0_2	P1	17	Port 0	ADDR	DATA
P0_3	P1	16	Port 0	ADDR	DATA
P0_4	P1	15	Port 0	ADDR	DATA
P0_5	P1	14	Port 0	ADDR	DATA
P0_6	P1	13	Port 0	ADDR	DATA
P0_7	P1	12	Port 0	ADDR	DATA
P0_8	P1	11	Port 2	ADDR	
P0_9	P1	10	Port 2	ADDR	
P0_10	P1	9	Port 2	ADDR	
P0_11	P1	8	Port 2	ADDR	
P0_12	P1	7	Port 2	ADDR	
P0_13	P1	6	Port 2	ADDR	
P0_14	P1	5	Port 2	ADDR	
P0_15	P1	4	Port 2	ADDR	
RESET	P2	19	RESET		
PSEN-	P2	18	PSEN		
ALE	P2	17	ALE		

8051-compatible Signal List for Timing Connectors

PIN NAME	E2415B POD	ANALYZER PIN	LABEL 1	LABEL 2	LABEL 3
P1_0	P3	19	PORT1	T2	
P1_1	P3	18	PORT1	T2EX	
P1_2	P3	17	PORT1	P1_2	
P1_3	P3	16	PORT1	P1_3	
P1_4	P3	15	PORT1	P1_4	
P1_5	P3	14	PORT1	P1_5	
P1_6	P3	13	PORT1	P1_6	
P1_7	P3	12	PORT1	P1_7	
P3_0	P3	11	PORT3	RXD	
P3_1	P3	10	PORT3	TXD	
P3_2	P3	9	PORT3	INT0	
P3_3	P3	8	PORT3	INT1	
P3_4	P3	7	PORT3	T0	
P3_5	P3	6	PORT3	T1	
P3_6	P3	5	PORT3	WR	
P3_7	P3	4	PORT3	RD	

Circuit board dimensions

The following figure gives the dimensions for the analysis probe. The dimensions are listed in inches and millimeters.



HP E2415B Dimensioons

Replaceable parts

The repair strategy for this analysis probe is board replacement. However, the table below lists some mechanical parts that may be replaced if they are damaged or lost. Contact your nearest Hewlett-Packard Sales Office for further information on servicing the board.

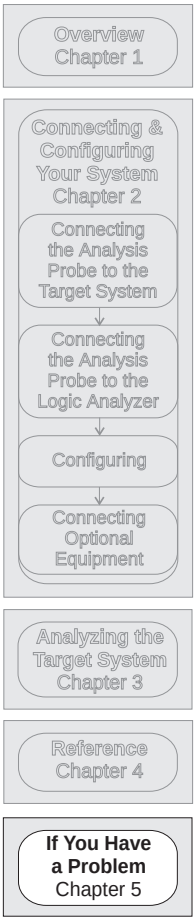
Exchange assemblies are available when a repairable assembly is returned to Hewlett-Packard. These assemblies have been set up on the "Exchange Assembly" program. This lets you to exchange a faulty assembly with one that has been repaired, calibrated, and performance verified by the factory. The cost is significantly less than that of a new assembly.

Replaceable Parts

HP Part Number	Description
E2415-66503	Circuit board assembly
E2415-68704	Inverse assembler disk pouch

If You Have a Problem

If You Have a Problem



Occasionally, a measurement may not give the expected results. If you encounter difficulties while making measurements, use this chapter to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions.

The information in this chapter is presented in the following sections:

- Logic analyzer problems
- Analysis probe problems
- Inverse assembler problems
- Intermodule measurement problems
- Messages
- Cleaning the instrument

If you still have difficulty after trying the suggestions in this chapter, contact your local Hewlett-Packard Service Center.

CAUTION

When you are working with the analyzer, be sure to power down both the analyzer and the target system before disconnecting or connecting cables, probes, and analysis probes. Otherwise, you may damage circuitry in the analyzer, analysis probe, or target system.

Analyzer Problems

This section lists general problems that you might encounter while using the analyzer.

Intermittent data errors

This problem is usually caused by poor connections, incorrect signal levels, or marginal timing.

- ☐ **Remove and reseat all cables and probes, ensuring that there are no bent pins on the analysis probe or poor probe connections.**
- ☐ **Adjust the threshold level of the data pod to match the logic levels in the system under test.**
- ☐ **Use an oscilloscope to check the signal integrity of the data lines.**

  Clock signals for the state analyzer must meet particular pulse shape and timing requirements. Data inputs for the analyzer must meet pulse shape and setup and hold time requirements.

See Also See "Capacitive loading" in this chapter for information on other sources of intermittent data errors.

Unwanted triggers

Unwanted triggers can be caused by instructions that were fetched but not executed.

- ☐ **Add the prefetch queue or pipeline depth to the trigger address to avoid this problem.**

  The logic analyzer captures prefetches, even if they are not executed. When you are specifying a trigger condition or a storage qualification that follows an instruction that may cause branching, an unused prefetch may generate an unwanted trigger.

No activity on activity indicators

- ☐ Check for loose cables, board connections, and analysis probe connections.
- ☐ Check for bent or damaged pins on the analysis probe.

No trace list display

If there is no trace list display, it may be that your trigger specification is not correct for the data you want to capture, or that the trace memory is only partially filled.

- ☐ Check your trigger sequencer specification to ensure that it will capture the events of interest.
- ☐ Try stopping the analyzer; if the trace list is partially filled, this should display the contents of trace memory.

Analyzer won't power up

If the logic analyzer power is powered down when it is connected to a powered-up target system, the logic analyzer may not be able to power up. Some logic analyzers are inhibited from powering up when they are connected to a target system that is already powered up.

- ☐ Disconnect all logic analyzer cabling from the analysis probe. This will allow the logic analyzer to power up. Reconnect logic analyzer cabling after power up.

Analysis Probe Problems

This section lists problems that you might encounter when using an analysis probe. If the solutions suggested here do not correct the problem, you may have a damaged analysis probe. Contact your local Hewlett-Packard Sales Office if you need further assistance.

Target system will not boot up

If the target system will not boot up after connecting the analysis probe, the microprocessor (if socketed) or the analysis probe may not be installed properly, or they may not be making electrical contact.

- ☐ **Ensure that you are following the correct power-on sequence for the analysis probe and target system.**

  1 Power up the analyzer and analysis probe.

  2 Power up the target system.

  If you power up the target system before you power up the analysis probe, interface circuitry in the analysis probe may latch up and prevent proper target system operation.

- ☐ **Verify that the microprocessor and the analysis probe are properly rotated and aligned so that the index pin on the microprocessor (pin 1 or pin A1) matches the index pin on the analysis probe.**

- ☐ **Verify that the microprocessor and the analysis probe are securely inserted into their respective sockets.**

- ☐ **Verify that the logic analyzer cables are in the proper sockets of the analysis probe and are firmly inserted.**

Erratic trace measurements

There are several general problems that can cause erratic variations in trace lists and inverse assembly failures.

- ☐ **Do a full reset of the target system before beginning the measurement.**

  Some analysis probe designs require a full reset to ensure correct configuration.

- ☐ **Ensure that your target system meets the timing requirements of the processor with the analysis probe installed.**

  See “Capacitive Loading” in this chapter. While analysis probe loading is slight, pin protectors, extenders, and adapters may increase it to unacceptable levels. If the target system design has close timing margins, such loading may cause incorrect processor functioning and give erratic trace results.

- ☐ **Ensure that you have sufficient cooling for the microprocessor.**

  Some microprocessors generate substantial heat. This is exacerbated by the active circuitry on the analysis probe board. You should ensure that you have ambient temperature conditions and airflow that meet or exceed the requirements of the microprocessor manufacturer.

Capacitive loading

Excessive capacitive loading can degrade signals, resulting in incorrect capture by the analysis probe, or system lockup in the microprocessor. All analysis probes add additional capacitive loading, as can custom probe fixtures you design for your application.

Careful layout of your target system can minimize loading problems and result in better margins for your design. This is especially important for systems that are running at frequencies greater than 50 MHz.

- ☐ **Remove as many pin protectors, extenders, and adapters as possible.**

- ☐ **If multiple analysis probe solutions are available, use one with lower capacitive loading.**

Inverse Assembler Problems

This section lists problems that you might encounter while using the inverse assembler.

When you obtain incorrect inverse assembly results, it may be unclear whether the problem is in the analysis probe or in your target system. If you follow the suggestions in this section to ensure that you are using the analysis probe and inverse assembler correctly, you can proceed with confidence in debugging your target system.

No inverse assembly or incorrect inverse assembly

This problem may be due to incorrect alignment, modified configuration files, incorrect connections, or a hardware problem in the target system. A locked status line can cause incorrect or incomplete inverse assembly.

- ☐ **Ensure that each logic analyzer pod is connected to the correct analysis probe connector.**

  There is not always a one-to-one correspondence between analyzer pod numbers and analysis probe cable numbers. Microprocessor interfaces must supply address (ADDR), data (DATA), and status (STAT) information to the analyzer in a predefined order. The cable connections for each analysis probe are often altered to support that need. Thus, one analysis probe might require that you connect cable 2 to analyzer pod 2, while another will require you to connect cable 5 to analyzer pod 2. See Chapter 2 for connection information.

- ☐ **Check the activity indicators for status lines locked in a high or low state.**

- ☐ **Verify that the STAT, DATA, and ADDR format labels have not been modified from their default values.**

  These labels must remain as they are configured by the configuration file. Do not change the names of these labels or the bit assignments within the labels. Some analysis probes also require other data labels. See Chapter 3 for more information.

- ☐ **Verify that all microprocessor caches and memory managers have been disabled.**

  In most cases, if the microprocessor caches and memory managers remain enabled you should still get inverse assembly. It may be incorrect because a portion of the execution trace was not visible to the logic analyzer.

- ☐ **Verify that storage qualification has not excluded storage of all the needed opcodes and operands.**

Inverse assembler will not load or run

You need to ensure that you have the correct system software loaded on your analyzer.

- ☐ **For the HP 16600/700 logic analysis systems, the inverse assembler must be installed on the hard drive using the procedures listed on the jacket for the CD ROM. Re-install the Processor Support Package for this product, then try loading the configuration file again.**

- ☐ **For other logic analyzers, ensure that the inverse assembler is on the same disk as the configuration files you are loading.**

  Configuration files for the state analyzer contain a pointer to the name of the corresponding inverse assembler. If you delete the inverse assembler, rename it, or use the File Manager Copy command to copy it to the HP 16600/700 logic analysis systems, the configuration process will fail to load the inverse assembler.

  See Chapter 3 for details.

Intermodule Measurement Problems

Some problems occur only when you are trying to make a measurement involving multiple modules.

An event wasn't captured by one of the modules

If you are trying to capture an event that occurs very shortly after the event that arms one of the measurement modules, it may be missed due to internal analyzer delays. For example, suppose you set the oscilloscope to trigger upon receiving a trigger signal from the logic analyzer because you are trying to capture a pulse that occurs right after the analyzer's trigger state. If the pulse occurs too soon after the analyzer's trigger state, the oscilloscope will miss the pulse.

- **Adjust the skew in the Intermodule menu.**

  You may be able to specify a skew value that enables the event to be captured.

- **Change the trigger specification for modules upstream of the one with the problem.**

  If you are using a logic analyzer to trigger the scope, try specifying a trigger condition one state before the one you are using. This may be more difficult than working with the skew because the prior state may occur more often and may not always be related to the event you are trying to capture with the oscilloscope.

Analyzer Messages

This section lists some of the messages that the analyzer displays when it encounters a problem.

". . . Enhanced Inverse Assembler Not Found"

This error only occurs on the HP 16600/700 logic analysis systems. This error occurs if you rename or delete the enhanced inverse assembler file that is attached to the configuration file, or if you do not properly install the inverse assembler file on the hard disk. Ensure that the inverse assembler file is not renamed or deleted. If you use the File Manager Copy command to copy an inverse assembler to the HP 16600/700 logic analysis systems, the enhanced inverse assembler will not load. Use the Install procedures listed on the jacket of the CD ROM to install the files for this product.

". . . Inverse Assembler Not Found"

This error occurs if you rename or delete the inverse assembler file that is attached to the configuration file. Ensure that the inverse assembler file is not renamed or deleted.

For the HP 16600/700 logic analysis systems, the inverse assembler must be installed on the hard drive using the procedures listed on the jacket for the CD ROM.

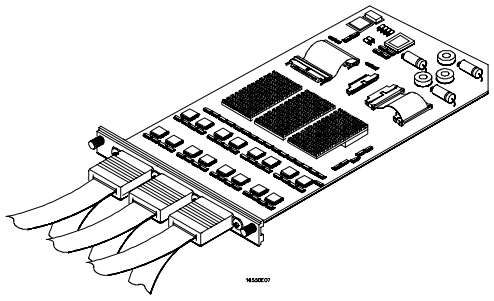
For other logic analyzers, if you have copied the files to the logic analyzer hard disk, ensure that the inverse assembler is located in the same directory as the configuration file.

". . . Does Not Appear to be an Inverse Assembler File"

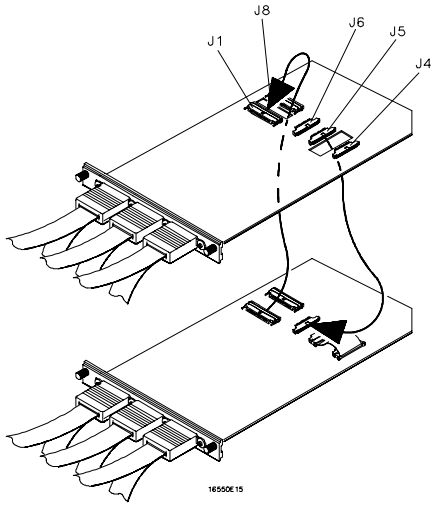
This error occurs if the inverse assembler file requested by the configuration file is not a valid inverse assembler. Use the Install procedures listed on the jacket of the CD ROM to re-install the files for this product.

"Measurement Initialization Error"

This error occurs when you have installed the cables incorrectly on logic analysis cards. The following diagrams show the correct cable connections for one-card and two-card HP 16550A installations. Ensure that your cable connections match the silk screening on the card, and that they are fully seated in the connectors. Then, repeat the measurement.



Cable Connections for One-Card HP 16550A Installations

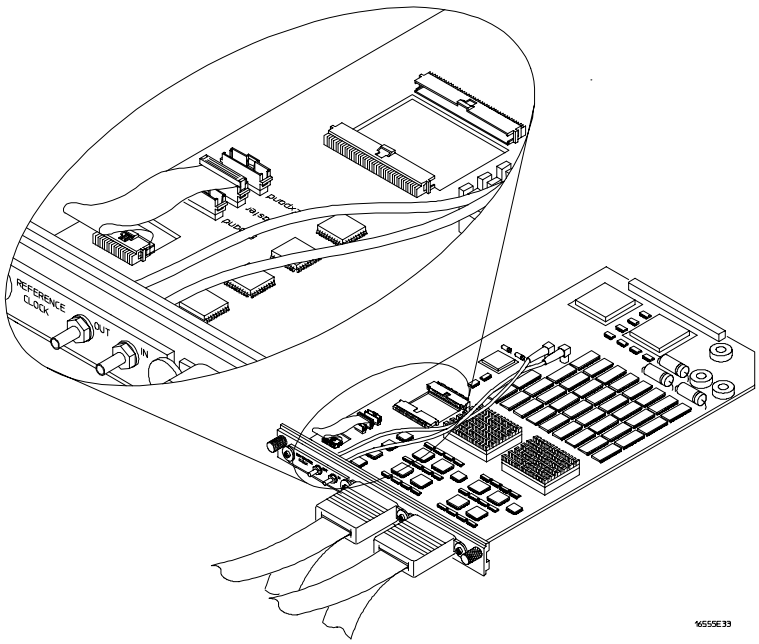


Cable Connections for Two-Card HP 16550A Installations

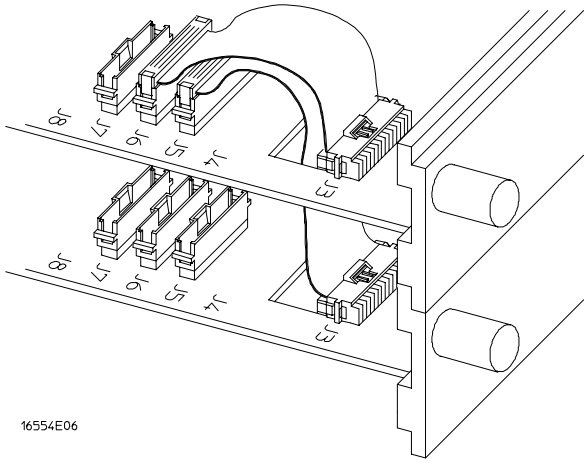
See Also

The *HP 16550A 100-MHz State/500-MHz Timing Logic Analyzer Service Guide*.

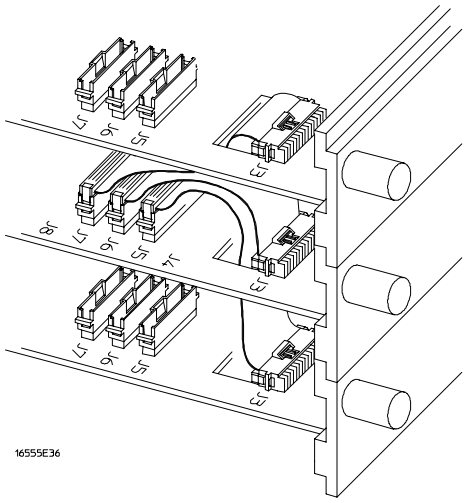
The following diagrams show the correct cable connections for one-card, two-card, and three-card installations on HP 16554A, HP 16555A/D, and HP 16556A/D logic analysis cards. Ensure that your cable connections match the silk screening on the card, and that they are fully seated in the connectors. Then, repeat the measurement.



Cable Connections for One-Card HP 16554/55/56 Installations



Cable Connections for Two-Card HP 16554/55/56 Installations



Cable Connections for Three-Card HP 16554/55/56 Installations

See Also

The HP 16554A 70-MHz State/250-MHz Timing Logic Analyzer Service Guide.

The HP 16555A 110-MHz State/250-MHz Timing Logic Analyzer Service Guide.

The HP 16556A 100-MHz State/400-MHz Timing Logic Analyzer Service Guide.

"No Configuration File Loaded"

This is usually caused by trying to load a configuration file for one type of module/system into a different type of module/system.

- ☐ Verify that the appropriate module has been selected from the Load {module} from File {filename} in the HP 16500A/B/C disk operation menu. Selecting Load {All} will cause incorrect operation when loading most analysis probe configuration files.

See Also Chapter 2 describes how to load configuration files.

"Selected File is Incompatible"

This occurs when you try to load a configuration file for the wrong module. Ensure that you are loading the appropriate configuration file for your logic analyzer.

"Slow or Missing Clock"

- ☐ This error message might occur if the logic analyzer cards are not firmly seated in the logic analysis system mainframe. Ensure that the cards are firmly seated.
- ☐ This error might occur if the target system is not running properly. Ensure that the target system is on and operating properly.
- ☐ If the error message persists, check that the logic analyzer pods are connected to the proper connectors on the analysis probe. See Chapter 2 to determine the proper connections.

“Time from Arm Greater Than 41.93 ms”

The state/timing analyzers have a counter to keep track of the time from when an analyzer is armed to when it triggers. The width and clock rate of this counter allow it to count for up to 41.93 ms before it overflows. Once the counter has overflowed, the system does not have the data it needs to calculate the time between module triggers. The system must know this time to be able to display data from multiple modules on a single screen.

“Waiting for Trigger”

If a trigger pattern is specified, this message indicates that the specified trigger pattern has not occurred. Verify that the triggering pattern is correctly set.

- When analyzing microprocessors that fetch only from word-aligned addresses, if the trigger condition is set to look for an opcode fetch at an address not corresponding to a word boundary, the trigger will never be found.

Cleaning the Instrument

If this instrument requires cleaning, disconnect it from all power sources and clean it with a mild detergent and water. Make sure the instrument is completely dry before reconnecting it to a power source.

Glossary

Analysis Probe A probe connected to the target microprocessor. It provides an interface between the signals of the target microprocessor and the inputs of the logic analyzer.

Connector Board A board whose only function is to provide connections from one location to another. One or more connector boards might be stacked to raise a probe above a target micoprocessor to avoid mechanical contact with other components installed close to the target microprocessor.

Elastomeric Probe Adapter A connector that is fastened on top of a target microprocessor using a retainer and knurled nut. The conductive elastomer on the bottom of the probe adapter makes contact with pins of the target microprocessor and delivers their signals to connection points on top of the probe adapter.

Emulation Module An emulation module is installed within the mainframe of a logic analyzer. It provides run control within an emulation and analysis test setup. See Emulation Probe.

Emulation Probe An emulation probe is a stand-alone instrument connected to the mainframe of a logic analyzer. It provides run control within an emulation and analysis test setup. See Emulation Module.

Flexible Adapter Two connection devices coupled with a flexible cable. Used for connecting probing hardware on the target microprocessor to the analysis probe.

General-purpose Flexible Adapter A cable assembly that connects the signals from an elastomeric probe adapter to an analysis probe. Normally, a male-to-male header or transition board makes the connections from the general-purpose flexible adapter to the analysis probe.

High-Density Adapter Cable A cable assembly that delivers signals from an analysis probe hardware interface to the logic analyzer pod cables. A high-density adapter cable has a single Mictor connector that is installed into the analysis probe, and two cables that are connected to corresponding odd and even logic analyzer pod cables.

High Density Termination Adapter Cable Same as a High Density Adapter Cable, except it has a termination in the Mictor connector.

Jumper Moveable direct electrical connection between two points.

Mainframe Logic Analyzer A logic analyzer that resides on one or more board assemblies installed in an HP 16500B/C, 1660xA, or 16700A mainframe.

Male-to-male Header A board assembly that makes point-to-point connections between the female pins of a flexible adapter or transition board and the female pins of an analysis probe.

Preprocessor Interface See Analysis Probe.

Preprocessor Probe See Analysis Probe.

Probe adapter See Elastomeric Probe Adapter.

Processor Probe See Emulation Probe and Emulation Module.

Prototype Analyzer The HP 16505A prototype analyzer acts as an analysis and display processor for the HP 16500B/C logic analysis system. It provides a windowed interface and powerful analysis capabilities.

Setup Assistant A software program that guides you through the process of connecting and configuring an analysis probe and logic analyzer to make measurements on a specific microprocessor.

Shunt Connector. See Jumper.

Stand-alone Logic Analyzer A stand-alone logic analyzer has a predefined set of hardware components which provide a specific set of capabilities. It is designed to perform logic analysis. A stand-alone logic analyzer differs from a mainframe logic analyzer in that it does not offer card slots for installation of additional capabilities, and its specifications are not modified based upon selection from a set of optional hardware boards that might be installed within its frame.

Transition Board A board assembly that obtains signals connected to one side and re-arranges them in a different order for delivery at the other side of the board.

1/4-Flexible Adapter An adapter that obtains one-quarter of the signals from an elastomeric probe adapter (one side of a target microprocessor) and makes them available for probing.

Index

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About this edition

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New editions are complete revisions of the manual. Many product updates do not require manual changes; and, conversely, manual corrections may be done without accompanying product changes. Therefore, do not expect a one-to-one correspondence between product updates and manual updates.